Datasheet

CONFIDENTIAL

IMPINJ E910, E710, E510, AND E310 RAIN RFID READER CHIPS

DATASHEET

Version 1.4

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OVERVIEW

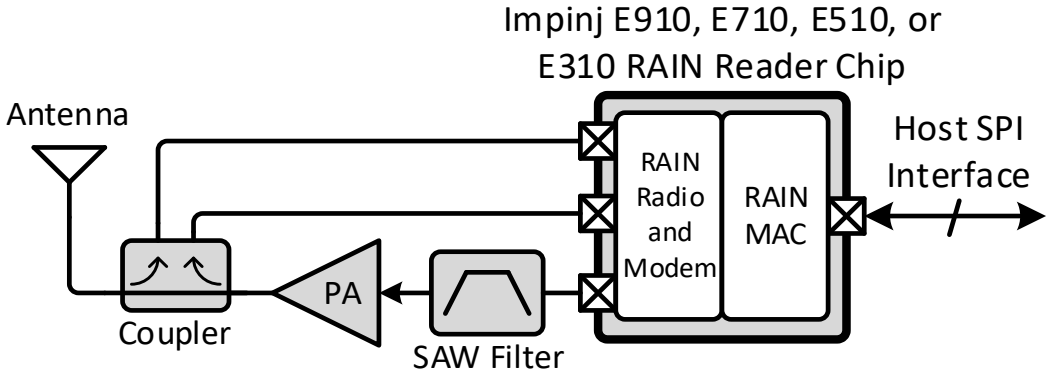
This document constitutes the confidential electrical, mechanical, and thermal specifications for the Impinj® E910, E710, E510, and E310 RAIN RFID reader chips. It contains a functional overview, mechanical characteristics, package signal locations, and targeted electrical specifications. For technical support, visit the Impinj support portal at support.impinj.com.

An overview of the capabilities of the Impinj E910, E710, E510, and E310 reader chips are shown in Table 1, and a reader system block diagram is shown in Figure 1.

Table 1: Impinj E910, E710, E510, and E310 Reader Chips Overview

Specification	Description
Air Interface Protocol	• EPCglobal® UHF Class 1 Gen 2 / ISO 18000-63 RFID • DSB-ASK, PR-ASK transmit modulation modes • Dense reader mode (DRM) supported
Chip Transmit Output Power	Configurable up to +11 dBm. (External power amplifiers supported for high performance applications, up to 33 dBm total Tx Power)
Chip Receive Sensitivity	• Impinj E910: -94 dBm • Impinj E710: -88 dBm • Impinj E510: -82 dBm • Impinj E310: -75 dBm Note: All values in FCC DRM RF Mode (20 µs TARI, 250 kHz BLF, Miller-4) at 1% PER with +7 dBm (Impinj E910) or +10 dBm (Impinj E710, E510, and E310) self-jammer
Tag Read Rates	• 1000+ tags per second Note: Impinj E910 or E710, in FCC fastest RF mode, FW v1.1+. See Table 12 for details.
Operating Frequencies	860 - 930 MHz
Supported Regions	All worldwide regions supported, including: • US, Canada, and other regions following US FCC 47 CFR Ch. 1 Part 15 • Europe and other regions following ETSI EN 302 208-1 (v3.3.1) • China, Japan, and other worldwide regions
Integration	RAIN Radio, Modem, MAC, RF Baluns, and Power Detectors included
Power	Low power consumption: (configuration dependent) • Active: 550 to 1000 mW • Idle: 28 to 55 mW • Disabled: 0.1 to 0.5 mW
Package	56-pin 6 mm x 6 mm sawn QFN, 0.85 mm thickness, 0.35 mm pitch

Figure 1 – Impinj Reader Chip-Based Circuit Block Diagram



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1 INTRODUCTION

Spanning a range of performance and price points, Impinj offers a comprehensive reader chip portfolio to identify, locate, and authenticate today's tens of billions of connected things, including retail apparel, pallets, parcels, pharmaceuticals, automotive parts, luggage, and much more. The Impinj E910, E710, E510, and E310 RAIN RFID reader chips are part of a portfolio of systems-on-chips (SoCs) built on the heritage of the Impinj Indy series that set performance standards for more than a decade. These new reader chips deliver:

- Up to 10 dB better receive sensitivity for reliable performance in new and existing use cases.
- 50% lower chip power consumption, supporting battery-powered, energy-efficient devices.
- Up to 80% smaller RAIN RFID system designs ideal for small, next-generation devices.
- Software- and pin-compatible designs for easy performance upgrades and design reuse.

The highly integrated Impinj E910, E710, E510, and E310 RAIN RFID reader chips are designed for EPC Gen2 / ISO18000-63 UHF RFID applications. The reader chips implement direct conversion receiver architecture, and operate in the worldwide UHF industrial, science, and medical (ISM) band. The reader chips contain all the RF and baseband blocks to interrogate and receive data from compatible RAIN tags, and an integrated microcontroller with embedded RAIN firmware providing the GS1 UHF Gen2 RAIN protocol as a pre-integrated feature.

1.1 Features

- Modem architecture uses modern digital signal processing
- Self-jammer cancellation (SJC) technology
- Fully integrated voltage-controlled oscillator (VCO) with worldwide RFID coverage
- Integrated Power Amplifier (PA) and baluns
- High compression point quadrature down-converting mixer
- Integrated radio-frequency (RF) envelope detectors for forward- and reverse-power sensing
- Integrated Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs)
- Configurable digital baseband
- Integrated ARM Cortex-M0+ microcontroller core with embedded firmware
- Host Serial Peripheral Interface (SPI) clocked at up to 4 MHz
- Impinj reader chip SDK including host library source code in C and code examples in C and python
- 6x6 mm package size

1.2 Reference Documents

The conventions used in the UHF Gen2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Impinj E910, E710, E510, and E310 RAIN RFID Reader Chip Datasheet. Users of this datasheet should familiarize themselves with the UHF Gen2 Specification.

The Impinj E910, E710, E510, and E310 reader chips are fully compliant with the protocol specifications and local regulation documents in Table 2:

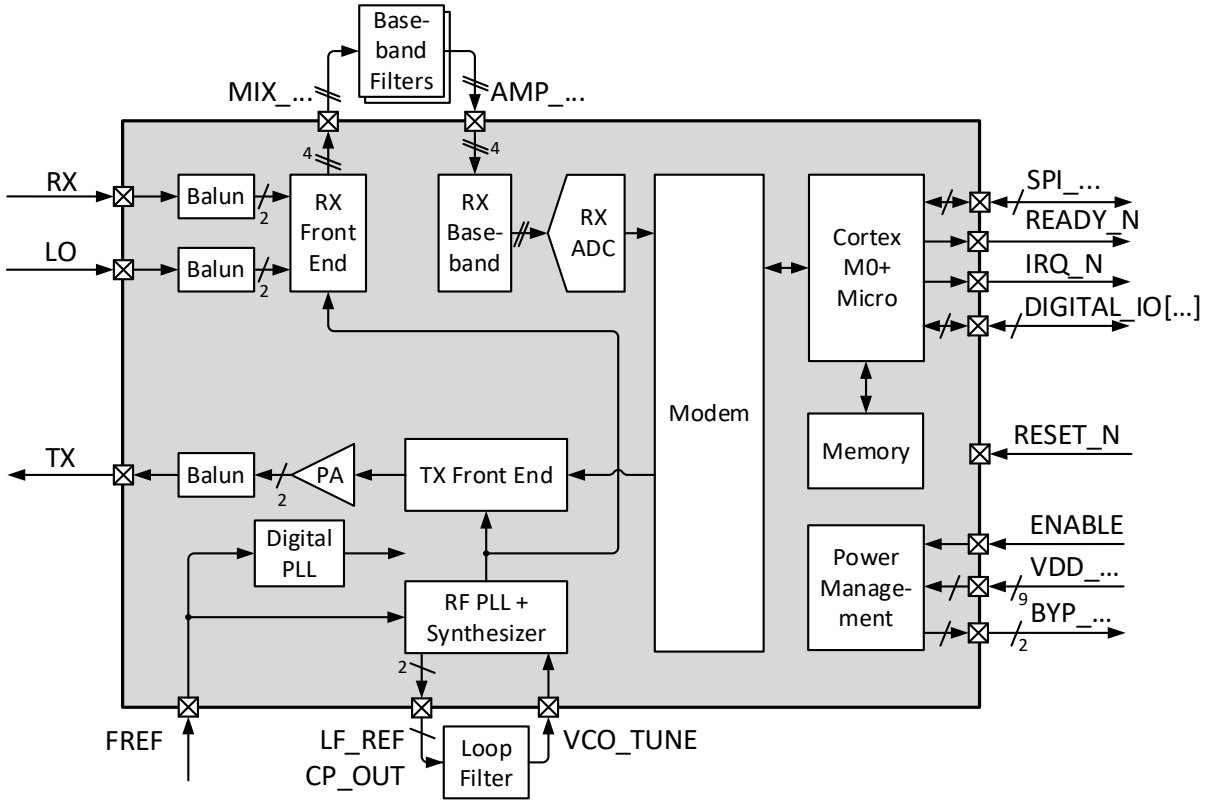
Table 2: Specification Documents

Protocol Specification Documents	Local Regulation Documents
• GS1 EPCGlobal Interoperability Test System for EPC compliant Class-1 Gen-2 UHF RFID	• FCC 47 CFR Ch. 1, part 15 • ETSI EN 302 208-1 v2.1.1

1.3 Block Diagram

Figure 2 contains a detailed internal block diagram of the Impinj E910, E710, E510, and E310 reader chips. The architecture is based on direct conversion for both the transmitter and receiver.

Figure 2 – Impinj Reader Chip Detailed Internal Block Diagram

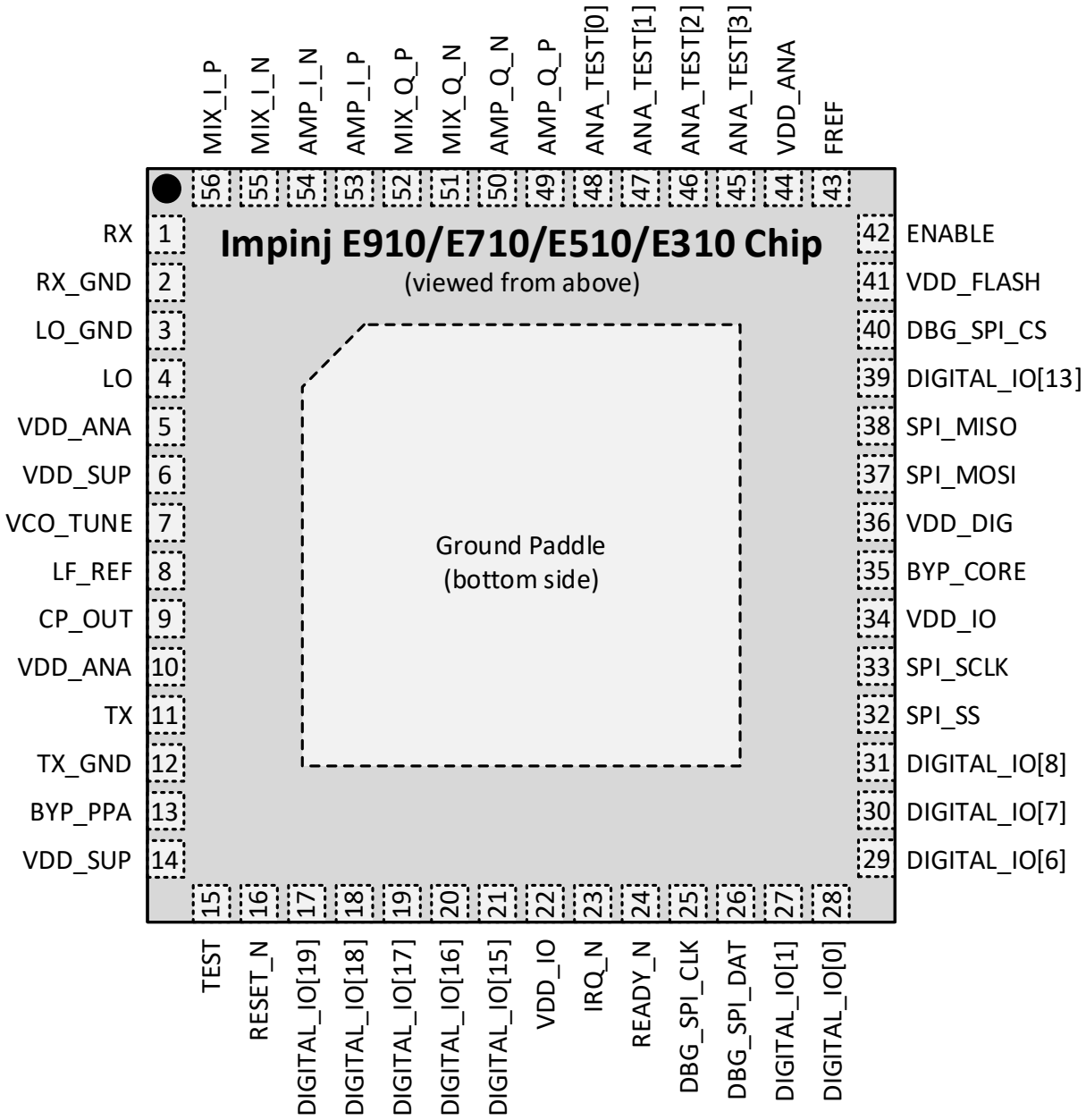


2 SPECIFICATIONS

2.1 Pin Listing and Signal Definitions

The Impinj E910, E710, E510, and E310 reader chips are offered in a 56-pin 6x6 mm QFN package. They require an external SAW filter and directional coupler in most configurations to implement a full radio circuit, along with a power amplifier (PA) if higher transmit power is required. The pinout for the 6x6 mm QFN is shown graphically in Figure 3 and in a list in Table 3. For package dimensions, see section 7.1 - Package Dimensions.

Figure 3 – Impinj Reader Chip Pinout



Note: Diagram not to scale

Table 3: Impinj Reader Chip Pin Signal Listing

Pin #	Pin Name	Type	Description
1	RX	RF In	RFID receive signal
2	RX_GND	RF Ground	RFID receive signal ground
3	LO_GND	RF Ground	RFID local oscillator/self-jammer cancellation reference signal ground
4	LO	RF In	RFID local oscillator/self-jammer cancellation reference signal
5	VDD_ANA	Power Supply	Analog power supply
6	VDD_SUP	Power Supply	Supervisory power supply
7	VCO_TUNE	Analog Input	VCO tuning input
8	LF_REF	Analog Output	PLL loop filter reference
9	CP_OUT	Analog Output	PLL charge pump output
10	VDD_ANA	Power Supply	Analog power supply
11	TX	RF Out	RFID transmit signal
12	TX_GND	RF Ground	RFID transmit signal ground
13	BYP_PPA	Power Bypass	Power amplifier power supply bypass
14	VDD_SUP	Power Supply	Supervisory power supply
15	TEST	DNU	Reserved for Impinj usage. Should be tied to ground.
16	RESET_N	Digital Input	Chip reset signal (active low)
17	DIGITAL_IO[19]	Digital IO	Digital input/output
18	DIGITAL_IO[18]	Digital IO	Digital input/output
19	DIGITAL_IO[17]	Digital IO	Digital input/output
20	DIGITAL_IO[16]	Digital IO	Digital input/output
21	DIGITAL_IO[15]	Digital IO	Digital input/output
22	VDD_IO	Power Supply	Digital input/output power supply
23	IRQ_N	Digital Output	Interrupt signal output (active low)
24	READY_N	Digital IO	Host SPI interface slave ready signal output (active low), boot to application/bootloader pin
25	DBG_SPI_CLK	Digital Output	Debug SPI interface master clock (SPI out for FW troubleshooting)
26	DBG_SPI_DAT	Digital Output	Debug SPI interface master MOSI (SPI out for FW troubleshooting)
27	DIGITAL_IO[1]	Digital IO	Digital input/output
28	DIGITAL_IO[0]	Digital IO	Digital input/output
29	STARTUP / DIGITAL_IO[6]	Digital IO	Digital input/output (must be pulled or driven high at startup)
30	DIGITAL_IO[7]	Digital IO	Digital input/output
31	DIGITAL_IO[8]	Digital IO	Digital input/output
32	SPI_SS	Digital Input	Host SPI interface slave select (active low)
33	SPI_SCLK	Digital Input	Host SPI interface clock
34	VDD_IO	Power Supply	Input/output power supply
35	BYP_CORE	Power Bypass	Core power supply bypass
36	VDD_DIG	Power Supply	Digital power supply
37	SPI_MOSI	Digital Input	Host SPI interface master output slave input
38	SPI_MISO	Digital Output	Host SPI interface master input slave output

Pin #	Pin Name	Type	Description
39	DIGITAL_IO[13]	Digital IO	Digital input/output
40	DBG_SPI_CS	Digital Output	Debug SPI interface master chip select (SPI out for FW troubleshooting)
41	VDD_FLASH	Power Supply	Flash memory power supply
42	ENABLE	Digital Input	Chip enable input
43	FREF	Clock Input	24 MHz PLL reference clock signal
44	VDD_ANA	Power Supply	Analog power supply
45	ANA_TEST[3]	Analog IO	Analog test signal
46	ANA_TEST[2]	Analog IO	Analog test signal
47	ANA_TEST[1]	Analog IO	Analog test signal
48	ANA_TEST[0]	Analog IO	Analog test signal
49	AMP_Q_P	Analog Input	Q post-mixer amplifier quadrature differential input (positive)
50	AMP_Q_N	Analog Input	Q post-mixer amplifier quadrature differential input (negative)
51	MIX_Q_N	Analog Output	Q mixer quadrature differential output (negative)
52	MIX_Q_P	Analog Output	Q mixer quadrature differential output (positive)
53	AMP_I_P	Analog Input	I post-mixer amplifier quadrature differential input (positive)
54	AMP_I_N	Analog Input	I post-mixer amplifier quadrature differential input (negative)
55	MIX_I_N	Analog Output	I mixer quadrature differential output (negative)
56	MIX_I_P	Analog Output	I mixer quadrature differential output (positive)
Paddle	GND	GND	Chip ground

2.2 IO Connections and Configurations

The Impinj E910, E710, E510, and E310 reader chips have input and output pins that are used to configure the devices. A host device such as an MCU or an application processor can control and monitor these pins. This section enumerates the required, recommended, and optional connections, and gives notes on their states.

Note: Impinj reader chip firmware versions 2.0 and earlier don't support using the DIGITAL_IO pins as inputs. This feature may be added in a future firmware release.

2.2.1 Digital IO Default Drive Modes

The Impinj E910, E710, E510, and E310 reader chip digital IOs start up in either a pull-up or pull-down drive mode. The DIGITAL_IOs can be reconfigured using the reader chip firmware operations, but at startup, their drive modes will be as shown in Table 4. The IO pull-up and pull-down resistance is specified in Table 19.

Table 4: Impinj Reader Chip Digital IO Default Drive Modes

Pin #	Pin Name	Type	Default Drive Mode
15	TEST	DNU	Pull-down
16	RESET_N	Digital Input	Pull-up
17	DIGITAL_IO[19]	Digital IO	Pull-up
18	DIGITAL_IO[18]	Digital IO	Pull-up
19	DIGITAL_IO[17]	Digital IO	Pull-up
20	DIGITAL_IO[16]	Digital IO	Pull-up
21	DIGITAL_IO[15]	Digital IO	Pull-up

Pin #	Pin Name	Type	Default Drive Mode
27	DIGITAL_IO[1]	Digital IO	Pull-up
28	DIGITAL_IO[0]	Digital IO	Pull-up
29	STARTUP / DIGITAL_IO[6]	Digital IO	Pull-up
30	DIGITAL_IO[7]	Digital IO	Pull-up
31	DIGITAL_IO[8]	Digital IO	Pull-up
39	DIGITAL_IO[13]	Digital IO	Pull-up

2.2.2 Host IO Connections

Table 5: Impinj Reader Chip Host Device Connections

Category	Pin Name	Type	Connection	Notes
SPI (Serial Peripheral Interface)	SPI_SS	Digital Input	Required	SPI slave select (active low) Required for SPI communication with the host.
	SPI_SCLK	Digital Input	Required	SPI clock Required for SPI communication with the host.
	SPI_MOSI	Digital Input	Required	SPI master output slave input Required for SPI communication with the host.
	SPI_MISO	Digital Output	Required	SPI master input slave output Required for SPI communication with the host.
	READY_N	Digital IO	Required	SPI slave ready signal output (active low), startup boot to application/bootloader pin Required for SPI communication with the host.
Reader Chip Control	ENABLE	Digital Input	Required	Chip enable input Allows host to control startup and put chip in a low power mode. Details on control below.
	RESET_N	Digital Input	Required	Chip reset signal (active low) Allows host to reset the reader chip without cycling the power. Must be sequenced as described in the next section. The reader chip drives this signal strong low during startup, so it must not be driven strong high externally.
Firmware State	IRQ_N	Digital Output	Recommended	Interrupt signal output (active low) Indicates to the host when data is ready on the reader chip. Can be left unconnected if host queries the reader chip regularly.

2.2.3 IO conditions

Certain Impinj E910, E710, E510, and E310 reader chip IOs must be in a specific electrical state for specific optional or mandatory operational states. They are listed below. These are in addition to the power supply pins, synthesizer pins, RF and baseband interface pins, etc. More details on startup sequence timing are shown in section 2.3.1 - Power Up Sequence.

ENABLE must be driven high to enable the reader chip. It should only be driven high after a stable 24 MHz clock signal is present at the FREF pin. ENABLE may be driven low to put the part into “Shutdown” mode, as described in section 3.7 - Power Modes.

RESET_N must be allowed to be driven low by the reader chip entering startup. If it is driven low to reset the part, it must be released >500 µs after the ENABLE pin is driven high. An internal pull-up resistor will pull the pin high. RESET_N may be used to reset the reader chips during operation.

DIGITAL_IO[6] must be driven high during reader chip firmware startup (after the RESET_N pin goes high, and before the READY_N pin goes low). This may be accomplished either by controlling the DIGITAL_IO[6] pin using a host device, or by applying a strong high or pullup voltage to the pin. If a pullup is applied, the

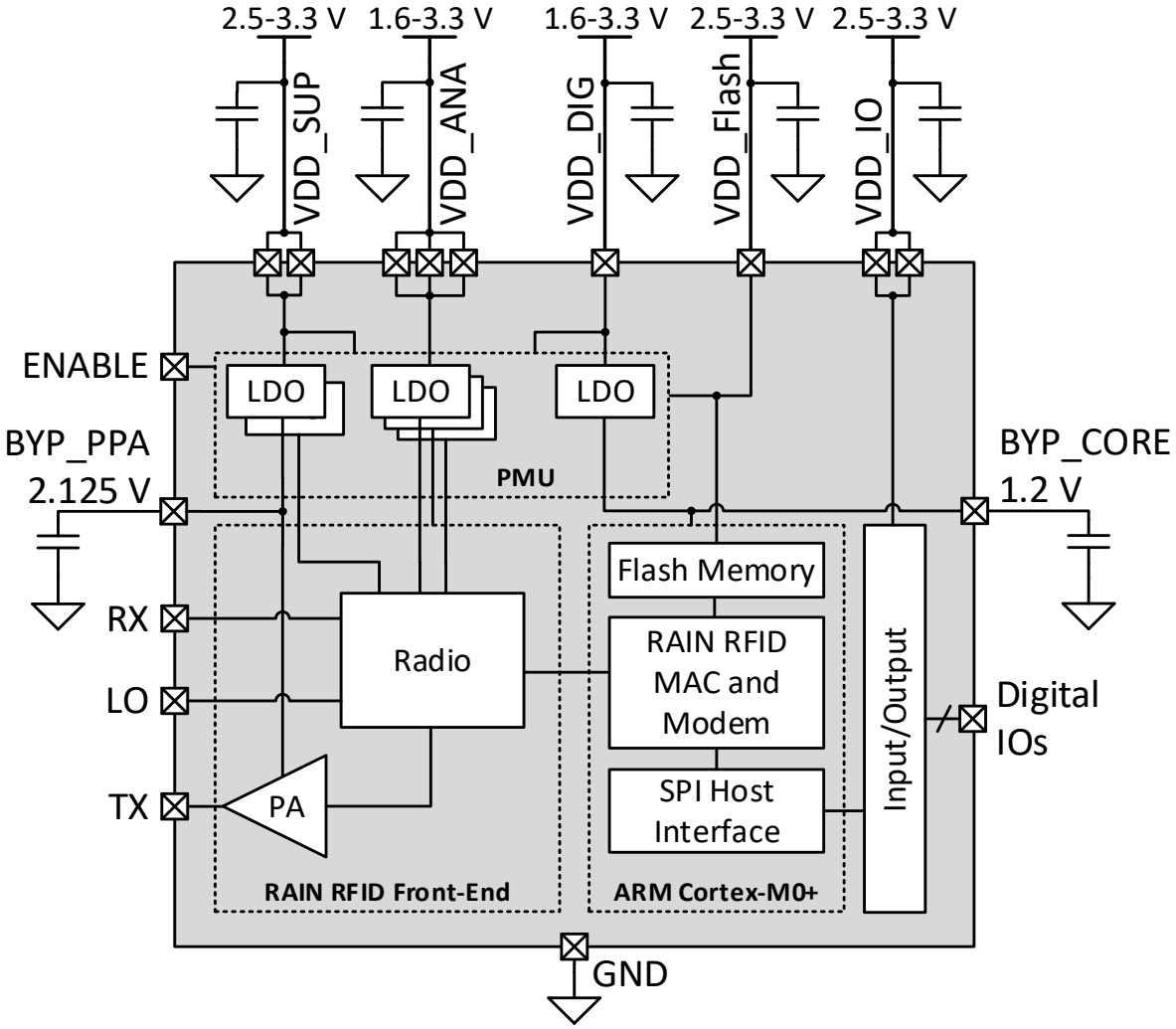
pin can be reconfigured as a strong drive by the reader chip and used to drive an external signal after startup is complete. On the Impinj E710 development board, this pin is pulled high with a 10 kΩ resistor.

READY_N must be driven strong low for 8706 FREF clock cycles (~362.75 µs) at startup (after the ENABLE pin goes high) to force the reader chip into bootloader mode. After a normal startup to application (not to bootloader) the READY_N pin will be driven low by E710 to indicate that startup has completed, and the reader chip is ready to communicate with the host via the SPI. Interface. The READY_N pin is also part of the SPI signaling wireline, as described in section 4.2 - SPI Digital Communication Interface.

2.3 Power Supply

The Impinj E910, E710, E510, and E310 reader chips have multiple power supply pins, and to achieve maximum performance, they must be properly configured. A block diagram of the reader chip's power supplies, their ranges, and the circuits they drive is shown in Figure 4.

Figure 4 – Impinj Reader Chip Power Supply Block Diagram



VDD_SUP, VDD_IO, and VDD_FLASH must all be powered at the same voltage, within the range of 2.5 to 3.3 volts. VDD_ANA and VDD_DIG must be powered at the same voltage, within the range of 1.6 to 3.3 volts, and lower than or equal to the VDD_SUP voltage. Note that these values are nominal, and the actual maximum and minimum values have additional margin, as shown in Table 7: Chip Operating Conditions.

All the supplies may share the same voltage, as long as it is within the shared range of 2.5 to 3.3 volts. Power consumption is optimized when each of the supplies are at their lowest allowed voltage (e.g. 1.6 volts for VDD_ANA and VDD_DIG, and 2.5 volts for VDD_SUP, VDD_IO, and VDD_FLASH). The valid range of supply voltage combinations is shown in Figure 5, and examples of both minimal power dual supply and a 3.3 V single supply are shown in Figure 6. Ferrite beads are used for isolation of the power supplies. These diagrams are simplifications, and both passive and active isolation of the power supplies can improve performance. See the Impinj E710 Development Board Application Note for more details.

Figure 5 – Impinj Reader Chip Valid Power Supply Voltage Conditions

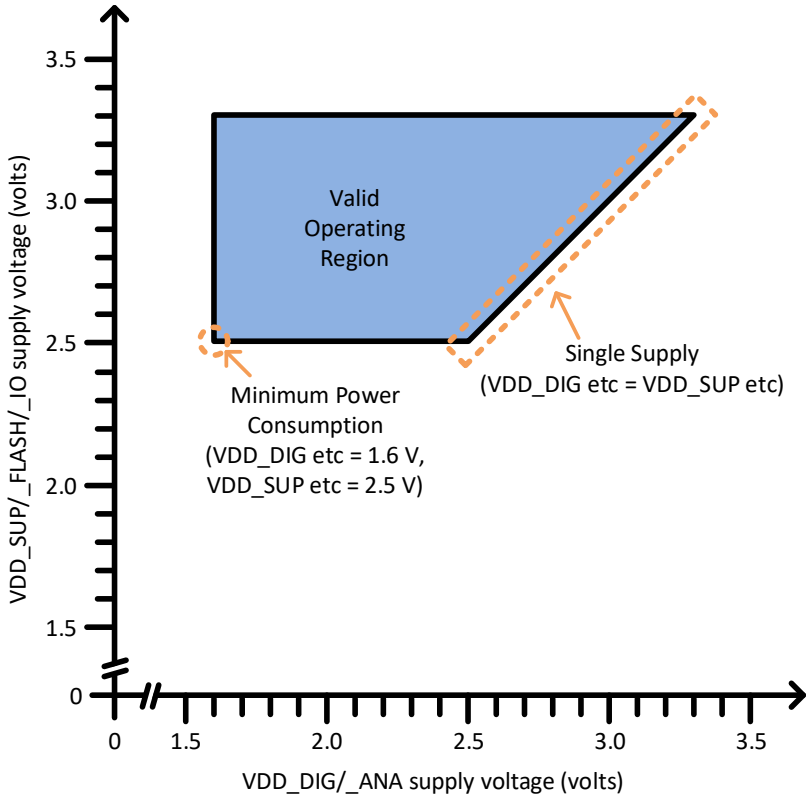
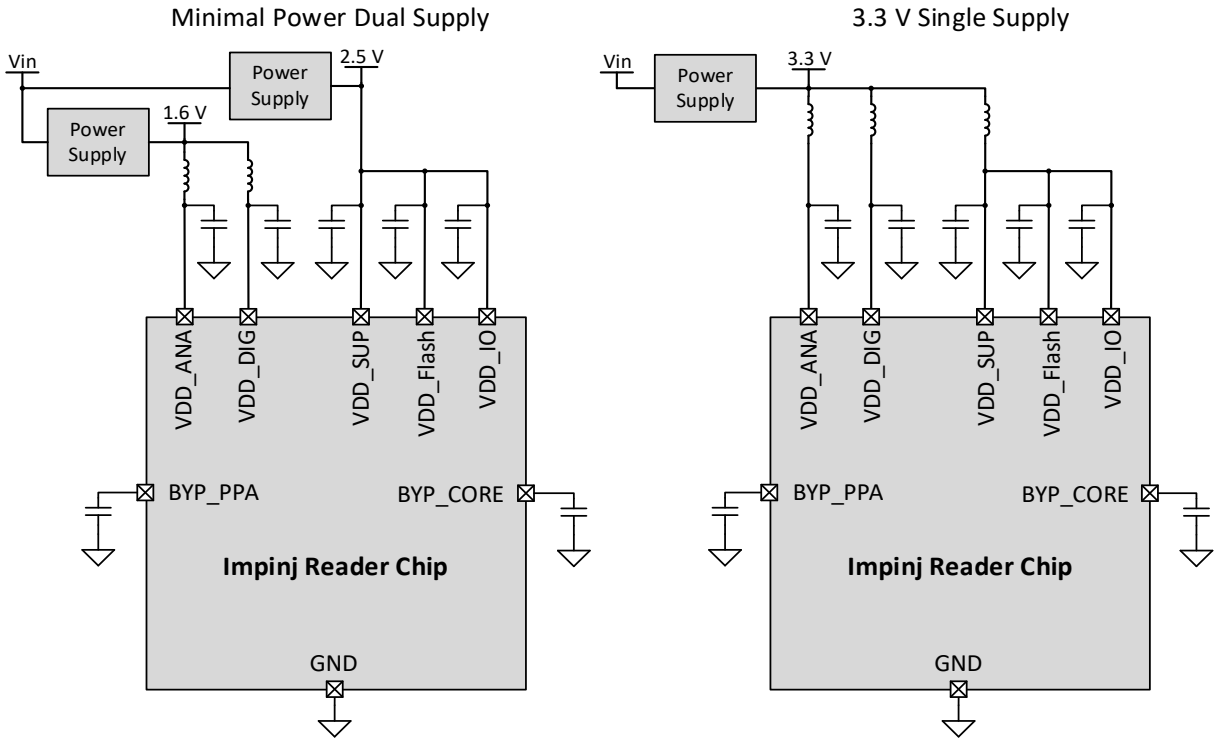


Figure 6 – Impinj Reader Chip Example Power Supply Configurations



The supply pins must be bypassed with external bypass capacitors. See the Impinj E710 Development Board Application Note for an example implementation. The individual bypass capacitors should be placed

close to the pins that they are bypassing. When an array of bypass capacitors is shown on the same net connecting multiple power pins, the array should be split up physically such that each pin has its own bypass capacitor.

BYP_PPA and BYP_CORE are not power supply inputs, but rather external bypass pins for the internally regulated power supplies. They should be externally bypassed with capacitance, but not driven. External bypass capacitance must be 10 µF or above, as demonstrated in the Impinj E710 development board. No external loads should be placed on these supply voltages. BYP_CORE is regulated to 1.2 V nominal. BYP_PPA is regulated to 2.125 V nominal. The un-bypassed, internal only analog supply BYP_ANA is regulated to 1.2 V nominal.

All of the duplicated power supplies (e.g. pins 6 and 14, both connected to VDD_SUP, see also VDD_ANA and VDD_IO) must be connected external to the reader chip.

For more details on potential external power supply implementations, see the Impinj E710 Development Board Application Note.

2.3.1 Power Up Sequence

The Impinj E910, E710, E510, and E310 reader chips must be powered up using a specific sequence of conditions on the power supplies, IOs, and other pins. This sequence is described verbally in the paragraph below, in a numbered list format following that, and graphically in Figure 7.

The power-up sequence must start by powering the VDD_SUP, VDD_IO, and VDD_FLASH supplies. The VDD_DIG and VDD_ANA power supplies may be powered at the same time or after the VDD_SUP, VDD_IO, and VDD_FLASH supplies. To reiterate, the VDD_DIG and VDD_ANA supplies must not be powered up before the other power supplies on the device. A 24 MHz clock must be present at FREF for the part to start up successfully. The part will not startup if the ENABLE pin is not high, or if the RESET_N pin is not allowed to be driven low by the reader chip. Approximately 500 µs after the enable pin goes high, the part will release the RESET_N pin, and firmware startup will begin. DIGITAL_IO[6] must be pulled or driven strong high during firmware startup, and then may be used as a digital input or output per application requirements. The READY_N pin will be driven low by the reader chip when firmware startup has completed, and the part is ready to communicate via SPI with the host device. The READY_N pin may also be driven low when RESET_N is released during startup to force the part into the bootloader mode. For more details on this, see section 2.2.3 - IO conditions.

This startup sequence is implemented in the Impinj reader chip SDK, specifically in **`power_transactor.c`** API **`ex10_power_up_to_application(…)`**.

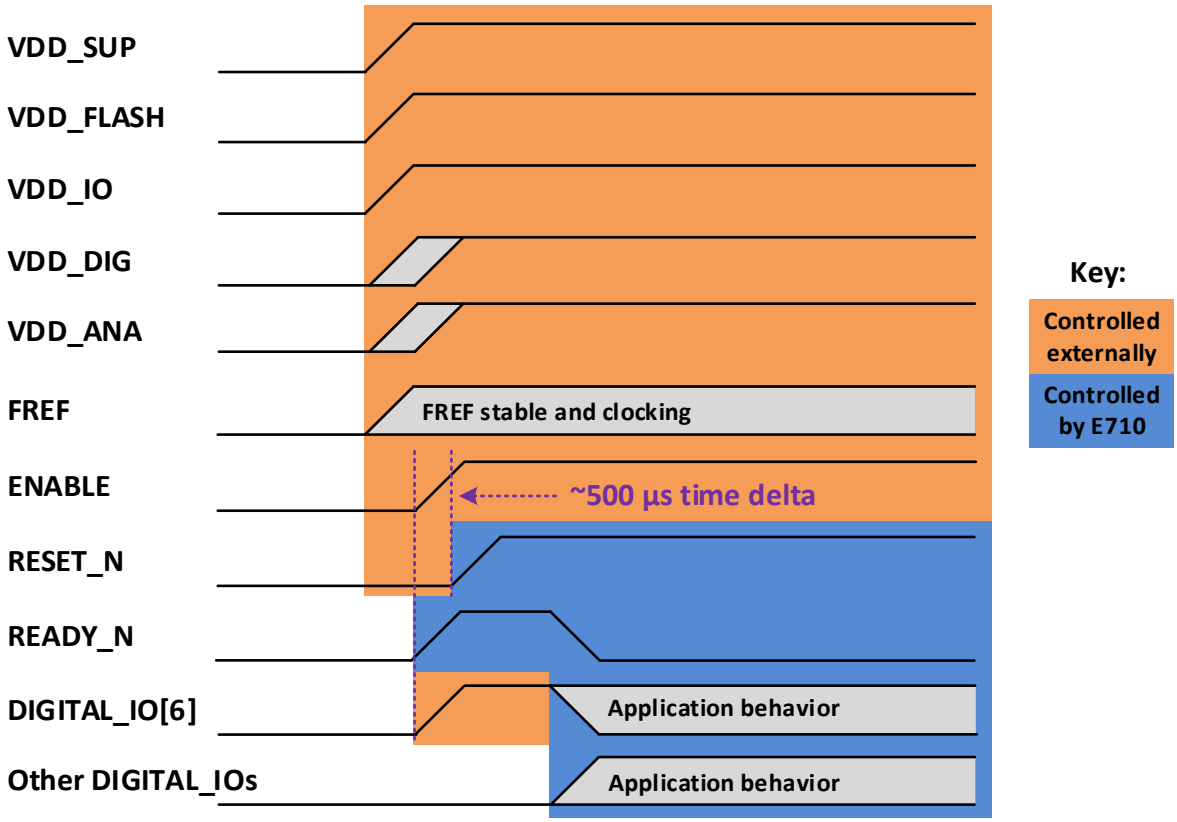
For more detail on startup, including detail on how to boot to the bootloader, see the firmware HTML documentation in the Impinj Ex10 Reader Chip SDK Specification.

1. Power the reader chip
    a. VDD_SUP, VDD_FLASH, and VDD_IO should be powered up before or simultaneously with VDD_DIG and VDD_ANA
    b. A 24 MHz clock signal should be applied to FREF simultaneously or after power is applied
2. After ~5 ms, Apply initial IO conditions to startup the reader chip
    a. RESET_N must be driven low by the host
    b. DIGITAL_IO[6] should be pulled high by the host
    c. ENABLE should be driven high by the host
    d. All other IOs should be left floating
3. After ~10 ms, apply final IO conditions to startup the reader chip
    a. RESET_N should be released by the host
    b. After approximately 500 µs, the RESET_N pin will be driven high by the reader chip, and firmware startup will begin
4. Observe the conclusion of startup
    a. When the READY_N pin is driven low by the reader chip, firmware startup has completed

b. At this point, the reader chip firmware will respond to SPI commands, and all the DIGITAL_IOs can be used for other purposes

c. The ENABLE pin should still be driven high, and RESET_N should be left floating during operation

Figure 7 – Impinj Reader Chip Startup Power Supply and IO Sequencing



2.3.2 Power Down Sequence

The Impinj E910, E710, E510, and E310 reader chips must be powered down in a specific sequence. That sequence is described in detail below and shown in Figure 8.

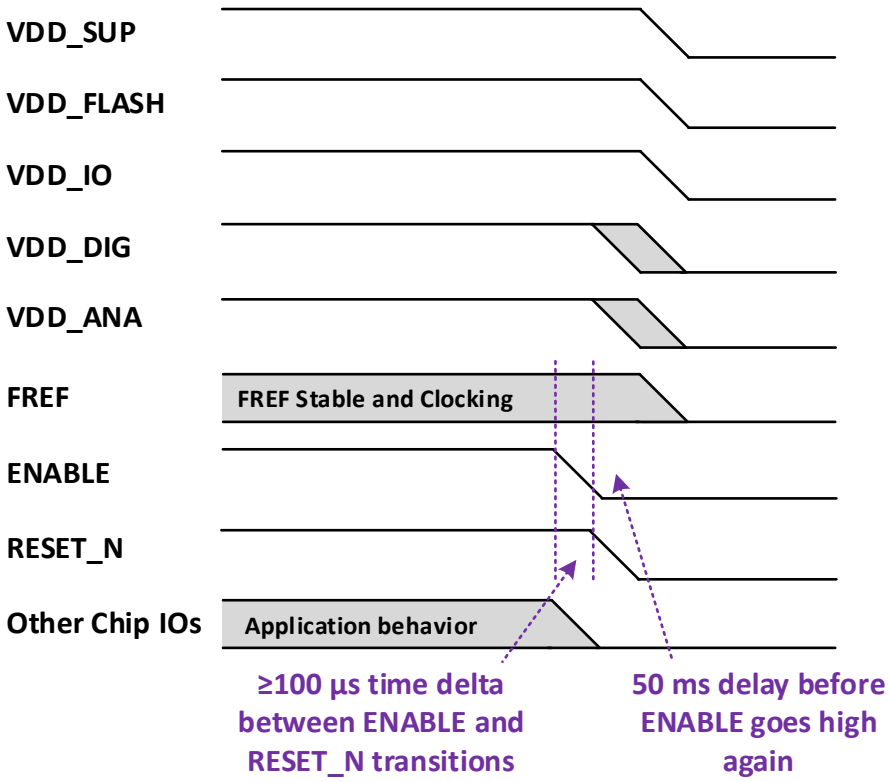
Note: It is critical that the ENABLE pin goes low 100 µs before RESET_N transitions low or power is removed from the reader chip. If this condition is not met, the reader chip could enter a state that is only recoverable through a reader chip power cycle.

1. Disable the reader chip
    a. The reader chip can be disabled by driving the ENABLE pin low
        i. At this point, the reader chip will stop responding to SPI communication, and application driven IO behaviors will cease
    b. The ENABLE pin must be driven low for 100 µs before the reader chip is reset or powered down
        i. The FREF input must continue clocking until this 100 µs delay has completed
2. Reset and power down the reader chip
    a. All chip IOs should either be left floating(high impedance) or driven to ground
    b. FREF may stop clocking
    c. The RESET_N pin may be driven low
    d. The VDD pins may be driven low, which will also drive RESET_N low if it is floating

i. VDD_DIG and VDD_ANA should be driven low either before or simultaneously with VDD_SUP, VDD_FLASH, and VDD_DIG

3. The reader chip should be left powered down for at least 50 ms before it is powered up again

Figure 8 – Impinj Reader Chip Power Down Sequence



2.3.3 Disable-Enable Sequence

The Impinj E910, E710, E510, and E310 reader chips must be disabled and re-enabled in a specific sequence. That sequence is described in detail below and shown in Figure 9.

The Disable functionality allows reduced power consumption without removing power from the reader chip. Reader designs should still maintain the ability to power down the reader chip to resolve unrecoverable states.

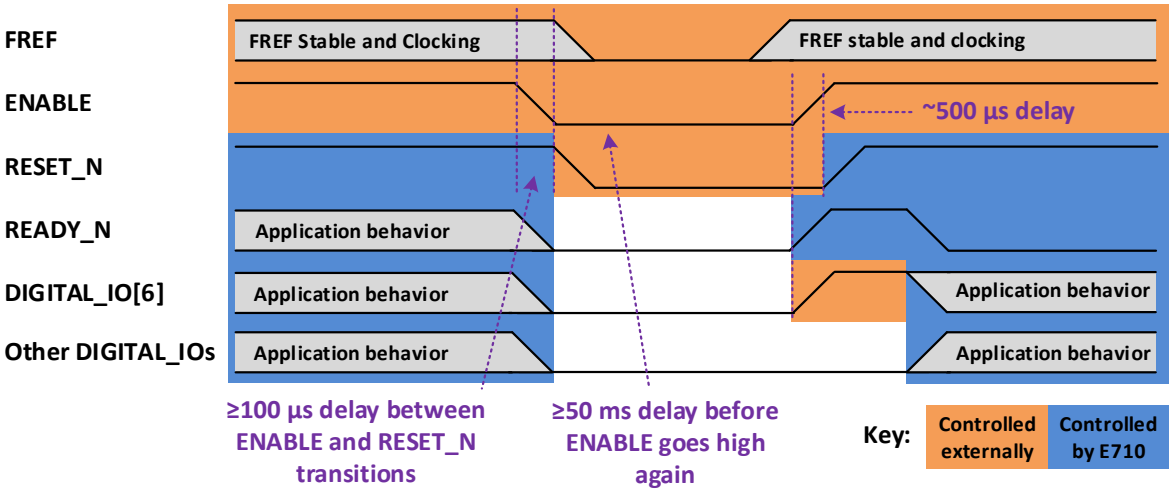
Note: It is critical that the ENABLE pin goes low 100 µs before RESET_N transitions low. If this condition is not met, the reader chip could enter a state that is only recoverable through a chip power cycle.

1. Disable the reader chip
    a. The reader chip should be disabled by driving the ENABLE pin low
        i. At this point, the reader chip will stop responding to SPI communication, and application driven IO behaviors will cease
    b. The ENABLE pin must be driven low for 100 µs before the RESET_N pin is driven low
        i. The FREF input must continue clocking until this 100 µs delay has completed
2. Reset the reader chip
    a. All chip IOs should either be left floating (high impedance) or driven to ground
    b. FREF may stop clocking
    c. The RESET_N pin should be driven low
3. Chip disabled
    a. At this point, the reader chip is disabled, and will consume reduced current

b. The reader chip must be left disabled for at least 50 ms before it is enabled again

4. After ~5 ms, Apply initial IO conditions to startup the reader chip
   a. RESET_N must be driven low by the host
   b. DIGITAL_IO[6] should be pulled high by the host
   c. ENABLE should be driven high by the host
   d. All other IOs should be left floating
5. After ~10 ms, apply final IO conditions to startup the reader chip
   a. RESET_N should be released by the host
   b. After approximately 500 µs, the RESET_N pin will be driven high by the reader chip, and firmware startup will begin
6. Observe the conclusion of startup
   a. When the READY_N pin is driven low by the reader chip, firmware startup has completed
   b. At this point, the reader chip firmware will respond to SPI commands, and all of the DIGITAL_IOs can be used for other purposes
   c. The ENABLE pin should still be driven high, and RESET_N should be left floating during operation

Figure 9 – Impinj Reader Chip Disable-Enable Sequence



2.4 Electrical Specifications

2.4.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 6 define the limitations for electrical and thermal stresses. These limits prevent permanent damage to the Impinj E910, E710, E510, and E310 reader chips. If the reader chip is exposed to conditions outside of these ranges, it is no longer guaranteed to operate properly or meet the performance specifications listed in this document, even after conditions return to the valid ranges.

Table 6: Absolute Minimum and Maximum Ratings

Parameter	Min	Max	Unit	Conditions
VDD_SUP/_FLASH/_IO voltage	-0.3	3.6	volts DC	
VDD_DIG/_ANA voltage	-0.3	3.6	volts DC	
Chip IO applied voltage	GND - 0.5	VDD_IO + 0.5	volts DC	Under typical conditions, IO voltages should not go below GND or above VDD_IO
ESD, Power supply and IO pins	N/A	N/A	N/A	HBM Class 3A
	N/A	N/A	N/A	CDM Class C2
ESD, RF pins	N/A	N/A	N/A	HBM Class 3A
	N/A	N/A	N/A	CDM Class C2
TX, LO, RX port RF input power	N/A	+20	dBm	Note: Optimal RF performance achieved at lower power levels, see Table 13
Storage Temperature	-55	125	°C	
Case Temperature	N/A	260	°C	For reflow purposes
Package Moisture Sensitivity Level	N/A	N/A	N/A	Moisture Sensitivity Level (MSL) 3

2.4.2 Operating Conditions

The operating conditions listed in this section describe the conditions under which the Impinj E910, E710, E510, and E310 reader chips will operate properly and meet the performance specifications listed in this document. If these conditions are not met, the reader chip will not perform as expected, but will also not suffer permanent damage.

Table 7: Chip Operating Conditions

Parameter	Min	Typ	Max	Unit	Conditions
VDD_SUP/_FLASH/_IO voltage	2.375	2.5 or 3.3	3.465	volts DC	All supplies in this row should be at the same voltage Typ column lists common voltages
VDD_DIG/_ANA voltage	1.52	1.6, 2.5, or 3.3	3.465	volts DC	All supplies in this row should be at the same voltage VDD_DIG must be ≤ VDD_SUP Typ column lists common voltages
Operating Ambient Temperature	-40	N/A	85	°C	Analysis performed using worst case power consumption, the θ_{JA} PCB layout and conditions
Junction Temperature		N/A	125	°C	
Junction to Ambient Thermal Resistance (θ_{JA})		27.8		°C/W	Typical 4-layer PCB layout, 9 vias below e-pad, no heat sink, no forced airflow

2.4.3 Radio Functional Specifications

Table 8: Chip Power Consumption

Parameter	Min	Typ	Max	Unit	Conditions
Chip performing inventory, transmitting at +11 dBm **Note: SJC does not increase power consumption.**	N/A N/A N/A N/A	950 700 650 550	1065 800 750 650	mW mW mW mW	3.3 V Single Supply 2.5 V Single Supply 3.3 / 1.6 V Dual Supply 2.5 / 1.6 V Dual Supply
Chip idle	N/A N/A N/A N/A	48 38 30 28	55 44 34 33	mW mW mW mW	3.3 V Single Supply 2.5 V Single Supply 3.3 / 1.6 V Dual Supply 2.5 / 1.6 V Dual Supply
Chip disabled	N/A N/A N/A N/A	0.4 0.1 0.3 0.1	0.5 0.2 0.4 0.2	mW mW mW mW	3.3 V Single Supply 2.5 V Single Supply 3.3 / 1.6 V Dual Supply 2.5 / 1.6 V Dual Supply
Chip held in reset	N/A		50	mW	Using RESET_N pin

Table 9: Chip Current Consumption Distribution

	VDD_ANA	VDD_DIG	VDD_FLASH	VDD_IO	VDD_SUP	Units
Power Supply Condition: Single supply 3.3 V						
Supply Voltage	3.3	3.3	3.3	3.3	3.3	Volts
Chip Active	133.8	34.3	0.0	0.1	115.0	mA
Chip Idle	0.4	10.2	0.0	0.1	3.8	mA
Chip Disabled	0.0	0.1	0.0	0.0	0.0	mA
Power Supply Condition: Single supply 2.5 V						
Supply Voltage	2.5	2.5	2.5	2.5	2.5	Volts
Chip Active	133.0	33.6	0.0	0.0	115.3	mA
Chip Idle	0.4	10.1	0.0	1.1	3.6	mA
Chip Disabled	0.0	0.0	0.0	0.0	0.0	mA
Power Supply Condition: Dual Supply 3.3 V / 1.6 V						
Supply Voltage	1.6	1.6	3.3	3.3	3.3	Volts
Chip Active	133.8	34.3	0.0	0.1	115.0	mA
Chip Idle	0.4	10.2	0.0	0.1	3.8	mA
Chip Disabled	0.0	0.1	0.0	0.0	0.0	mA
Power Supply Condition: Dual Supply 2.5 V / 1.6 V						
Supply Voltage	1.6	1.6	2.5	2.5	2.5	Volts
Chip Active	133	33.6	0.0	0.0	115.3	mA
Chip Idle	0.4	10.1	0.0	1.1	3.6	mA
Chip Disabled	0.0	0.0	0.0	0.0	0.0	mA

Note: All values typical, rounded to the nearest tenth of a mA

Table 10: Chip Radio Overall Specifications

Parameter	Min	Typ	Max	Unit	Conditions
Forward Link Modulation	N/A	N/A	N/A		DSB-ASK PR-ASK
Forward Link TARI	6.25	N/A	25	µs	Reader modes in FW limit specific values
PIE Ratio	1.5	N/A	2.0		Reader modes in FW limit specific values
Backward Link Frequency (BLF)	40	N/A	640	kHz	Reader modes in FW limit specific values

Table 11: Impinj Reader Chip Reader Mode IDs and Parameters

Old Mode ID	FCC Mode ID	ETSI LB Mode ID	ETSI UB Mode ID	Supported Regions*	Mode Optimization	Forward Link Modulation	Tari (µs)	PIE	BLF (kHz)	Back-scatter Link Modulation
N/A	**103**	N/A	N/A	FCC	FCC Read Rate	DSB-ASK	6.25	1.5	640	FM0
11	102	N/A	**302**	ETSI UB+	ETSI UB Read Rate	PR-ASK	7.5	2.0	640	FM0
N/A	**120**	N/A	N/A	FCC	FCC Hybrid	PR-ASK	6.25	1.5	640	Miller M=2
N/A	N/A	**203**	N/A	Japan	Japan Read Rate	PR-ASK	12.5	1.5	426	FM0
1	124	N/A	**323**	ETSI UB+	ETSI UB Hybrid	PR-ASK	7.5	2.0	640	Miller M=2
N/A	N/A	**226**	N/A	Japan	Japan Hybrid	PR-ASK	12.5	1.5	426	Miller M=2
N/A	N/A	**202**	N/A	ETSI LB+	ETSI LB Read Rate	PR-ASK	15	1.5	426	FM0
N/A	N/A	**225**	N/A	ETSI LB+	ETSI LB Hybrid	PR-ASK	15	2.0	426	Miller M=2
N/A	148	N/A	**345**	ETSI UB+	ETSI UB Hybrid	PR-ASK	7.5	1.5	640	Miller M=4
15	147	N/A	**344**	ETSI UB+	ETSI UB DRM	PR-ASK	7.5	2.0	640	Miller M=4
12	125	**223**	325	ETSI LB+	ETSI LB Hybrid	PR-ASK	15	2.0	320	Miller M=2
3	123	**222**	324	ETSI LB+	ETSI LB Hybrid	PR-ASK	20	2.0	320	Miller M=2
5	141	**241**	342	ETSI LB+	ETSI LB DRM	PR-ASK	20	2.0	320	Miller M=4
7	146	**244**	343	ETSI LB+	FCC DRM	PR-ASK	20	2.0	250	Miller M=4
13	185	**285**	382	ETSI LB+	Sensitivity	PR-ASK	20	2.0	160	Miller M=8

*Supported Regions column indicates which regions a mode should pass regulatory certification tests on the Impinj E710 Development Board. The listed region is the most difficult region to pass, indicating that less difficult regions will also pass. For example, Mode 302 will pass ETSI upper band, and also FCC, but not ETSI lower band.

Table 12: Impinj Reader Chip Reader Mode Performance

Mode ID*	Mode Optimization	Forward Link Modulation	Tari (µs)	PIE	BLF (kHz)	Back-scatter Link Modulation	Chip Receive Sensitivity Maximum** (dBm)				Typical Optimized Read Rate*** (tags/s)
							E910	E710	E510	E310	
103	FCC Read Rate	DSB-ASK	6.25	1.5	640	FM0	-84	-78	N/A	N/A	1000+
302	ETSI UB Read Rate	PR-ASK	7.5	2.0	640	FM0	-84	-78	N/A	N/A	800+
120	FCC Hybrid	PR-ASK	6.25	1.5	640	Miller M=2	-87	-81	-75	N/A	700+
203	Japan Read Rate	PR-ASK	12.5	1.5	426	FM0	-85.5	-79.5	N/A	N/A	650+
323	ETSI UB Hybrid	PR-ASK	7.5	2.0	640	Miller M=2	-87	-81	-75	N/A	550+
226	Japan Hybrid	PR-ASK	12.5	1.5	426	Miller M=2	-88.5	-82.5	-76.5	N/A	500+

Mode ID*	Mode Optimization	Forward Link Modulation	Tari (µs)	PIE	BLF (kHz)	Back-scatter Link Modulation	Chip Receive Sensitivity Maximum** (dBm)				Typical Optimized Read Rate*** (tags/s)
							E910	E710	E510	E310	
202	ETSI LB Read Rate	PR-ASK	15	1.5	426	FM0	-85.5	-79.5	N/A	N/A	500+
225	ETSI LB Hybrid	PR-ASK	15	2.0	426	Miller M=2	-88.5	-82.5	-76.5	N/A	400+
345	ETSI UB Hybrid	PR-ASK	7.5	1.5	640	Miller M=4	-90	-84	-75	N/A	400+
344	ETSI UB DRM	PR-ASK	7.5	2.0	640	Miller M=4	-90	-84	-78	N/A	400+
223	ETSI LB Hybrid	PR-ASK	15	2.0	320	Miller M=2	-90	-84	-78	-71	300+
222	ETSI LB Hybrid	PR-ASK	20	2.0	320	Miller M=2	-90	-84	-78	-71	250+
241	ETSI LB DRM	PR-ASK	20	2.0	320	Miller M=4	-93	-87	-81	-74	200+
244	FCC DRM	PR-ASK	20	2.0	250	Miller M=4	-94	-88	-82	-75	150+
285	Sensitivity	PR-ASK	20	2.0	160	Miller M=8	-99	-93	-87	-80	50+

*Reader mode availability shown for Impinj Reader Chip SDK+FW version 2.0. For a full listing of reader modes and parameters, see Table 11

**1% Packet Error Rate, with +7 dBm self-jammer at Impinj E910 RX pin or +10 dBm self-jammer at Impinj E710, E510, or E310 RX pin, DC blocking baseband filter (not DRM), typical Gen2 parameters

***Tag read rates shown are for a large tag population in a quiet RF environment, using the Impinj E710 Development Board. Read rates for Impinj E910 reader chip are typically higher, and Impinj E510 and E310 reader chips are typically lower.

Note: For information on selecting a Reader Mode, see the following support article: https://impinj.zendesk.com/hc/en-us/articles/4408250378387

Table 13: Chip Receiver Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input frequency	860		930	MHz	RX and LO Ports
Input impedance		50		ohm	RX and LO ports
Return loss	10			dB	S11 RX and LO Ports
IIP2 – In Band		+51		dBm	Receiver RF Front End
IIP2 – Out of Band		+56		dBm	Receiver RF Front End
IIP3 – In Band		+13		dBm	Receiver RF Front End
IIP3 – Out of Band		+9		dBm	Receiver RF Front End
E910 RX port self-jammer power			+8	dBm	Must also be 10 dB or more below LO port input power
E710, E510, E310 RX port self-jammer power			+11	dBm	Must also be 7 dB or more below LO port input power
LO port input power			+18	dBm	**Note:** Some applications may see better performance with a lower LO port input power
RX sensitivity		See Table 12			
RSSI measurement accuracy		3		dB	After per-board RSSI calibration

Parameter	Min.	Typ.	Max.	Unit	Conditions
Phase measurement accuracy		+/- 5		degrees	Phase measurements have 180 degrees of phase ambiguity in non-FM0 modes

Table 14: Chip Transmitter Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Maximum TX power output capability	+11			dBm	Chip is guaranteed to produce ≥ +11 dBm in its highest power configuration
TX output power regulatory compliant range	+5		+11	dBm	Across this chip output power range, regulatory compliance is guaranteed with external amplification up to the maximum power allowed in the region Below this range, reader overall output power must be reduced by 1 dB per 1 dB of chip transmit power to meet regulatory compliance For more detail, see the TX Path Attenuation section in the Impinj E710 Development Board Application Note
TX output power analog dynamic range	30			dB	**Note:** Optimal spectral performance is achieved at maximum chip TX power. See section 3.1 for details.
TX port analog power step size	N/A	1	N/A	dB	**Note:** Digital power control offers finer control
TX power digital control resolution		12		Signed bits	Linear control, full scale achieves maximum TX output power For more detail, see the Impinj E910, E710, E510, and E310 Based Reader Calibration Application Note

Table 15: Chip Power Detectors

Parameter	Min.	Typ.	Max.	Unit	Conditions
RX and LO power detector input	-15	N/A	+18	dBm	
RX and LO power detector accuracy		+/- 0.5		dB	After calibration Input power +4 to +17 dBm
		+/- 1.0		dB	After calibration Input power -6 to +4 dBm

Table 16: Chip Transmit Synthesizer

Parameter	Min.	Typ.	Max.	Unit	Conditions
Frequency range	860	N/A	930	MHz	
Frequency grid		100 125 250		kHz kHz kHz	Europe (ETSI 302 208) EU1, EU2, Japan, China, Korea USA (FCC)
Reference input frequency		24		MHz	TCXO Specification
Reference frequency tolerance			10	ppm	TCXO Specification
Reference input level	0.5		1.5	Vp-p	AC Coupled clipped sine wave Alternate waveforms require external filtering, see section 3.6.1
PLL settling time		1.5		ms	100 kHz grid, recommended PLL loop filter configuration
TX Phase noise		-120		dBc/Hz	Δf = 250 kHz
		-136		dBc/Hz	Δf = 1 MHz

Parameter	Min.	Typ.	Max.	Unit	Conditions
		-139		dBc/Hz	Δf = 3.7 MHz
TX In-band spurious emissions		-77		dBc	RBW = 3 kHz, average detector
TX Out-of-band spurious emissions		-42 -39 -6		dBm dBm dBm	Lower ETSI band, RBW = 120 kHz, peak detector Upper ETSI band, RBW = 120 kHz, peak detector Above 960 MHz (FCC) RBW = 1 MHz, average detector
TX carrier second harmonic		-30		dBc	
TX carrier third harmonic		-25		dBc	
TX Clock harmonic spurs		-87.6 -83.6		dBc dBc	At 864 MHz At 960 MHz Assuming 96 MHz digital clock
TX Clock sideband spurs		-80		dBc	+/- digital clock frequency (96 MHz) from carrier frequency

2.4.4 Auxiliary Analog Specifications

Table 17: Chip Auxiliary ADC Specifications

Parameter	Typ	Unit	Conditions
Input Minimum	0	Volts	
Input Maximum	1	Volts	
Resolution	10	Bits	Full scale
DNL	2	LSB	
INL	4	LSB	
Input Impedance	10	kohms	Measured relative to ground
Sample Rate	100	ksps	Limited by host communication rate

Table 18: Chip Auxiliary DAC Specifications

Parameter	Typ	Unit	Conditions
Resolution	10	Bits	
Current Mode Output Minimum	0	µA	
Current Mode Output Maximum	100	µA	
Current Mode DNL	2	LSB	
Current Mode INL	2	LSB	

2.4.5 IO Functional Specifications

Table 19: Chip Digital IO Specifications

Parameter	Min	Typ	Max	Unit	Conditions
Input high voltage	2		VDD_IO	V	Input high voltage levels
Input low voltage	-0.3		0.8	V	Input low voltage levels
Output high voltage	VDD_IO - 0.1			V	Output high voltage
Output low voltage			0.4	V	Output low voltage
Output sink and source current	4			mA	

Parameter	Min	Typ	Max	Unit	Conditions
IO pull up resistance	34	51	81	kohms	

2.4.6 Host SPI Interface Functional Specifications

Table 20 contains the requirements of the host SPI interface. For more details on SPI configuration, see section 4.2.

Table 20: Chip Host SPI Interface Specifications

Parameter	Min	Typ	Max	Unit
SPI Host Clock SCLK Frequency – Application	1.00	3.80	4.00	MHz
SPI Host Clock SCLK Frequency – Bootloader	0.90	0.95	1.00	MHz
SPI Host Clock SCLK Rise/Fall Time	330			ps
SPI Host Clock SCLK Duty Cycle	40	50	60	%
SPI Host Chip Select CS Setup Time	30			ns
SPI Host Chip Select CS Hold Time	3			ns
SPI Host Data Output MOSI Setup Time	30			ns
SPI Host Data Output MOSI Hold Time	3			ns
SPI Host Data Input MISO Valid Time			13	ns

3 FUNCTIONAL DESCRIPTION

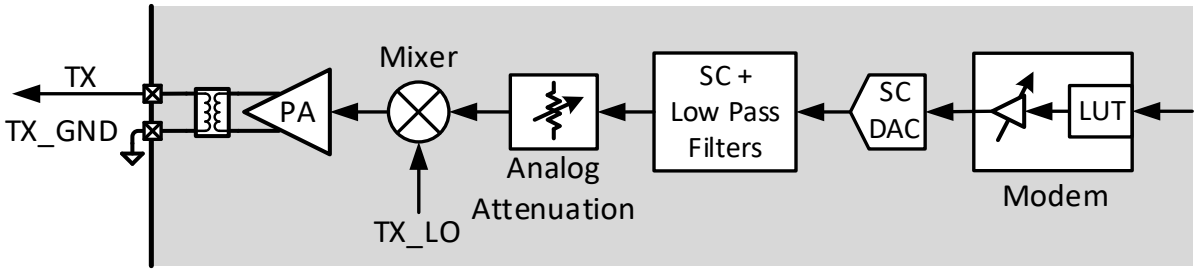
3.1 Analog Transmitter Path

The Impinj E910, E710, E510, and E310 reader chips contain the entire digital and analog TX signal chain required to transmit up to the maximum transmit power of the reader chips, as specified in Table 14: Chip Transmitter Specifications. This signal chain is shown in Figure 10. An external power amplifier may be used in applications where additional transmit power is required.

The transmitted waveform is generated inside the modem, where a lookup table contains a sequence of digital values. Those digital values go through a digital multiplication with a signed 12-bit gain value (also known as “fine gain”). After the digital multiplication, the values enter a switched capacitor (SC) digital to analog converter (DAC), and exit as an analog waveform. The analog waveform goes through switched cap and low pass filters before an analog attenuation stage. The analog attenuation (also known as “gross gain”) has 30 ~1 dB attenuation steps. After attenuation, the analog waveform is mixed with the transmit local oscillator (TX_LO), and then amplified by the internal PA, and finally output through a balun as a single ended signal on the TX pin.

The Impinj E910, E710, E510, and E310 reader chips produce optimal spectral performance when the internal power amplifier is operated at the maximum allowable power (~11 dBm). The internal analog and digital gain can be reconfigured at runtime to cover a wide power range. Given the optimal spectral performance at high output power, the reader chip and surrounding circuitry, including external PA bias, should be configured to target maximum reader output power at the maximum chip output power. Then the overall output power can be reduced to lower values by reducing the internal chip analog gain. For more details on optimizing transmit power, including selecting external TX attenuation circuit values, see the Impinj E710 Development Board Application Note.

Figure 10 – Transmitter Front End Analog Circuitry



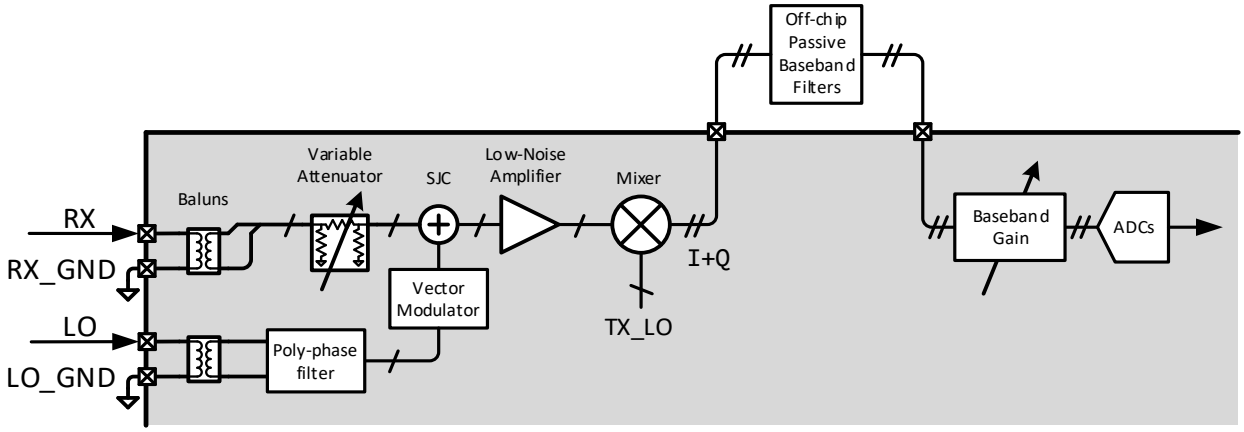
3.2 Analog Receiver Data Path

3.2.1 Receiver Front End Circuitry

The Receive (RX) and Local Oscillator (LO) RF inputs to the Impinj E910, E710, E510, and E310 reader chips are single ended, meaning no external balun is required to convert a single ended PCB trace signal to a differential signal for connection to the reader chip. Local RF ground signals are exposed at the adjacent pins (RX_GND and LO_GND), to optimize RF performance.

The Impinj E910, E710, E510, and E310 reader chip internal receiver circuitry is shown in Figure 11.

Figure 11 – Receiver Front End Analog Circuitry



3.2.2 Local Oscillator Input

The Local Oscillator (LO) input has a maximum input power, as described in Table 13: Chip Receiver Specifications. This means that in designs with high transmit powers, external attenuation may be required to reduce the incident power on the LO port. See the Impinj E710 Development Board Application Note for more details.

3.2.3 Self-Jammer Cancellation Block

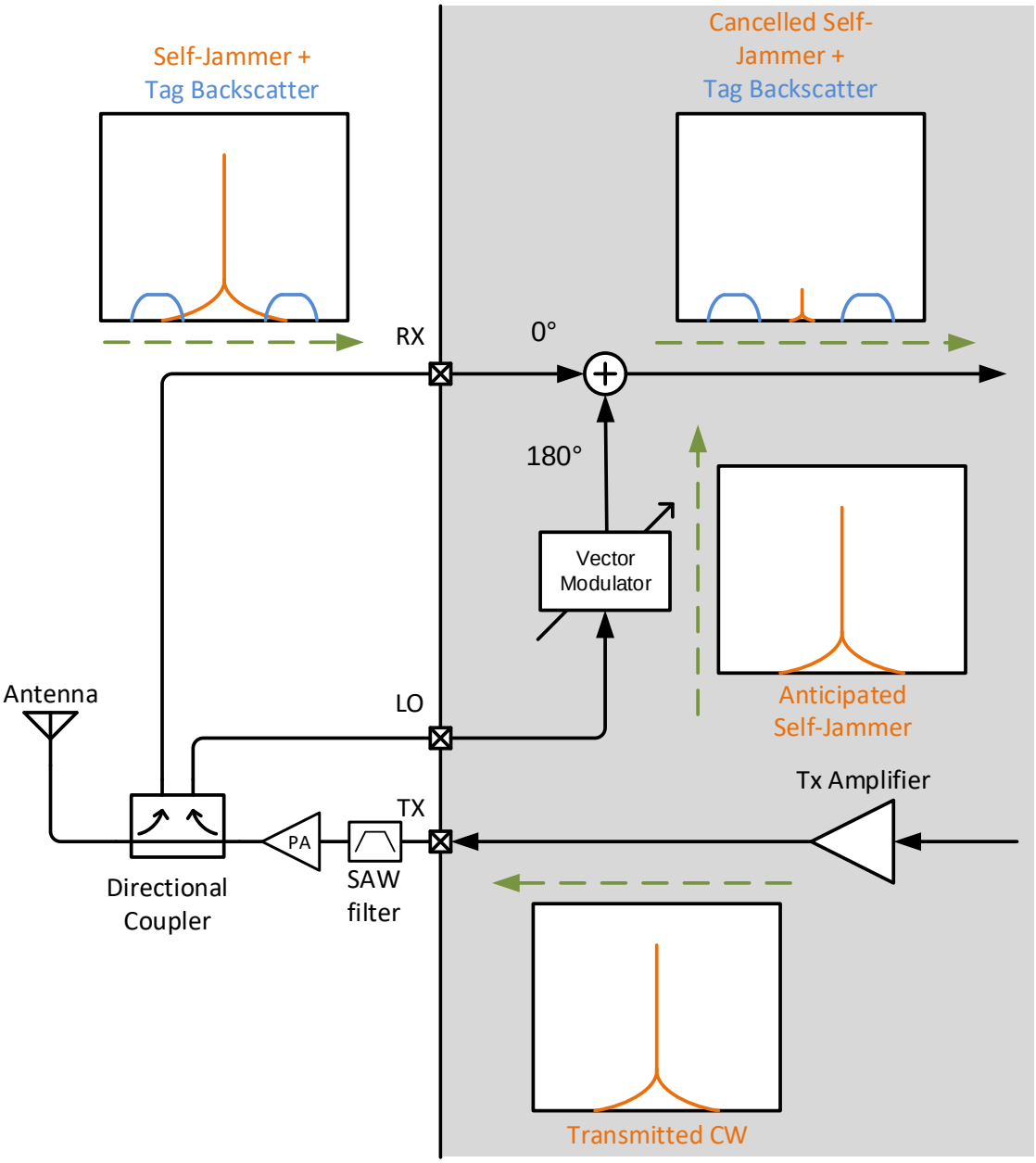
The Impinj E910, E710, E510, and E310 reader chips contain self-jammer cancellation (SJC) circuitry to improve receiver sensitivity. This circuit effectively reduces the negative impact of antenna reflection of the transmitted carrier wave (CW) on the receiver's sensitivity. RAIN systems using monostatic antenna configurations suffer from self-jammer problems because the transmitter must transmit CW continuously while the tags are backscattering their reverse link signal. That transmitted CW will reflect off of the antenna, resulting in a self-jammer signal incident at the receive port of the reader chip. That self-jammer signal will be much larger in amplitude than the reverse link signal from the tags.

The next-generation SJC block in the Impinj E910, E710, E510, and E310 reader chips iterate upon the SJC block developed in the Impinj Indy R2000 chip, reducing current consumption by implementing passive self-jammer cancellation, and improving sensitivity by increasing the resolution of the vector modulator circuit.

The Impinj E910, E710, E510, and E310 reader chips perform self-jammer cancellation by converting the Local Oscillator (LO) signal into an anticipated reflected CW and subtracting it from the Receive (RX) signal, using the Vector Modulator and other components shown in Figure 11. An example of the complete signal chain and resultant receive signal spectrum is shown in Figure 12.

Proper operation of the SJC requires that the LO signal have the proper amplitude as it enters the Impinj E910, E710, E510, and E310 reader chips, as shown in the electrical specs in Table 13: Chip Receiver Specifications. In most applications, this will require the use of additional passive attenuation outside of the reader chip. For examples of this circuit configuration, see the Impinj E710 Development Board Application Note.

Figure 12 – Self Jammer Cancellation Spectrum



3.2.4 Receive Baseband Interface

After the self-jammer signal is removed from the receive signal, the resulting RF signal is demodulated using the LO, resulting in a quadrature baseband signal. This signal is then filtered to remove out of band frequency content. The unfiltered signal is output from the reader chip on the differential quadrature MIX_... pins, and after external passive baseband filtration, it re-enters the reader chip through the differential quadrature AMP_... pins. The filtered baseband signal is then further amplified and filtered inside the reader chip, and finally digitized in on-chip ADCs to be processed by the modem. This arrangement is shown in Figure 13.

The component topology and values for the off-chip baseband filters vary by application. For recommendations, see the Impinj E710 Development Board Application Note. In some configurations, baseband signal filtering is not required, but in all cases the design should have at minimum DC blocking capacitors to interface between the receive mixer and the amplifiers before the ADC.

The reader chips have a single set of differential quadrature input and output pins, so if multiple passive filter networks are desired, external RF switching must be added to the circuit, as shown in the Impinj E710 development board.

The individual mixer output and amplifier input pins each have a configurable series resistor inside the part, with a resistance of either 250 or 1000 Ω, as configured by the firmware using the field **`HpfMode`** in register **`HpfOverrideSettings`**. This is shown in Figure 14.

Impinj's implementation of the SDK uses the 250 Ω resistance to match the 500 Ω characteristic impedance baseband filters implemented on the Impinj E710 development board.

Figure 13 – Receive Baseband Interface

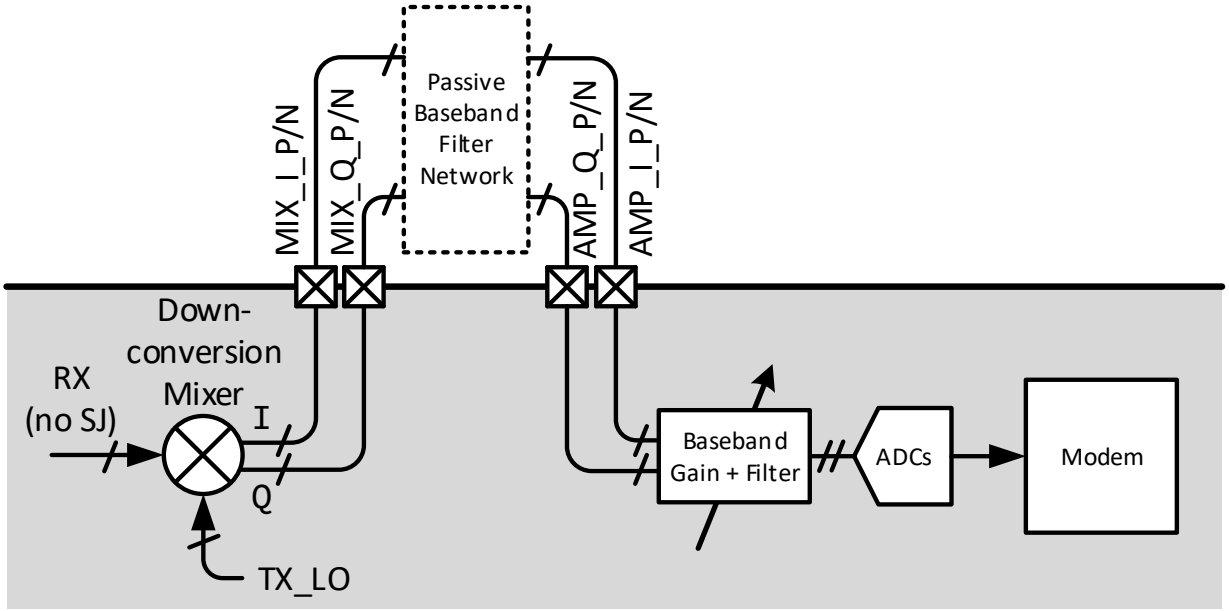
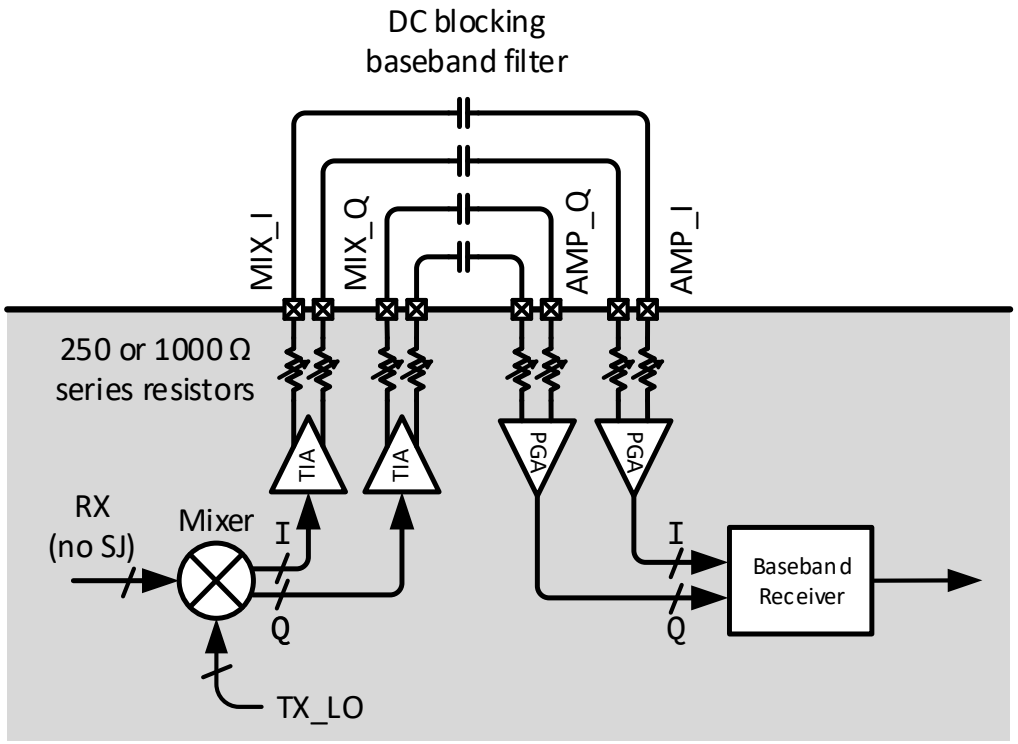


Figure 14 – Receiver Baseband Filter Pin Interface Detail



3.3 Antenna Configuration Scenarios

The Impinj E910, E710, E510, and E310 reader chips can be configured for monostatic (single antenna used for both transmit and receive) or bistatic (separate antennas used for transmit and receive) operation. Monostatic configurations are generally more popular, because of the lower cost and size of a single antenna system, but bistatic configurations have the advantage of increased receive sensitivity due to the smaller self-jammer signal on the receive antenna.

The Impinj E910, E710, E510, and E310 reader chips can also be configured for operation with multiple monostatic antennas, for example in a system with multiple physical zones, each with their own antennas. This can be accomplished using an external RF switch, also known as a multiplexer (mux), at the transmitted port of the directional coupler. The RF switch can be controlled by specific GPIOs. This arrangement is shown in Figure 17.

Figure 15 – Monostatic Antenna Configuration

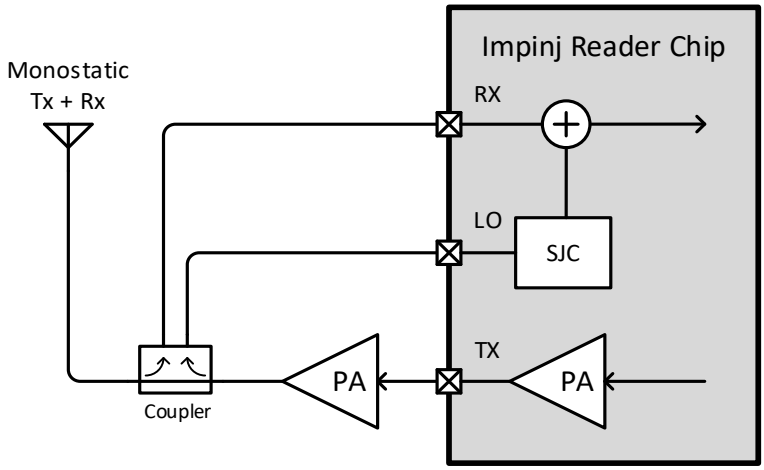


Figure 16 – Bistatic Antenna Configuration

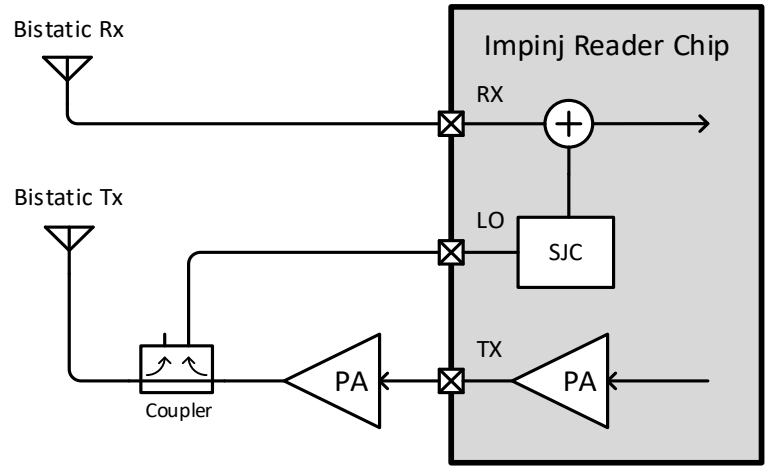
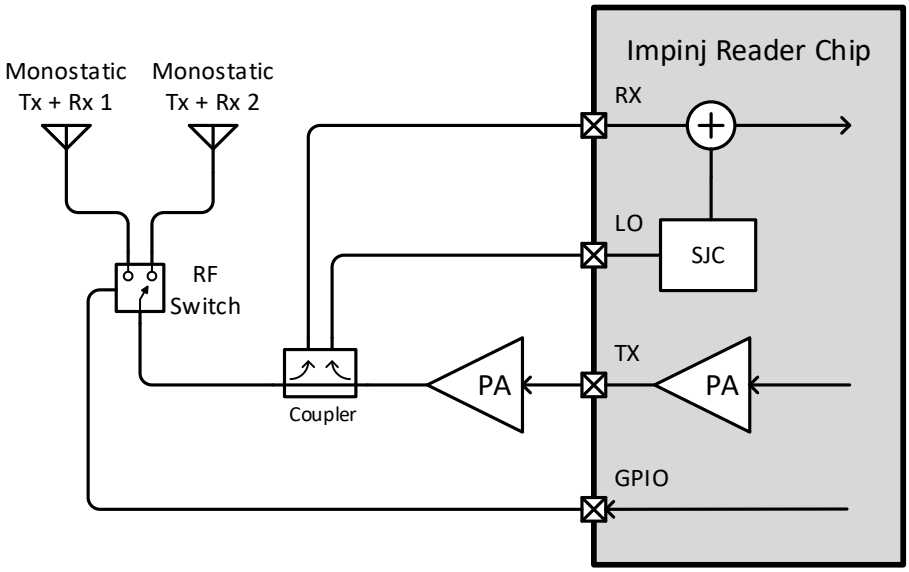


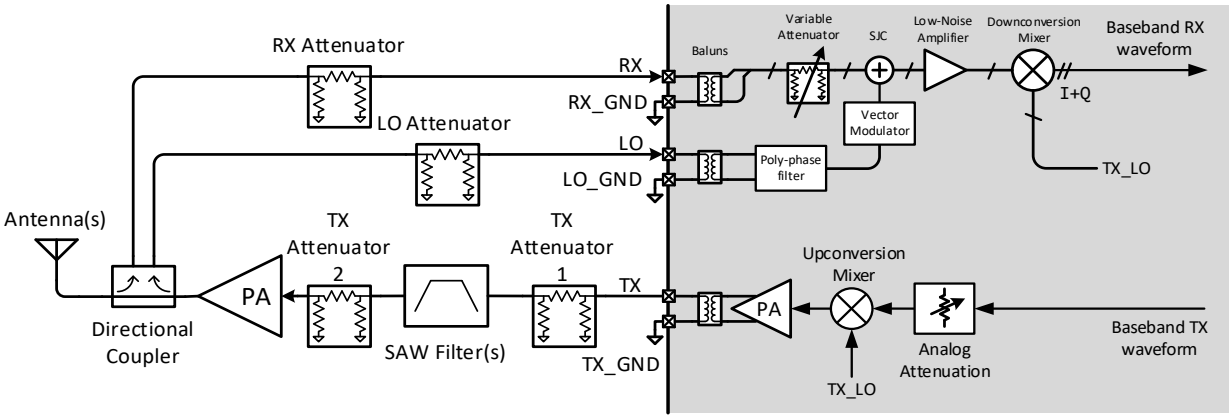
Figure 17 – Multiple Monostatic Antennas With RF Switch



3.4 RF TX, LO, and RX Path Configuration

The Impinj E910, E710, E510 and E310 reader chips' transmit (TX), local oscillator (LO), and receive (RX) pins must be connected to the antenna(s) via RF Front End circuitry to successfully implement a RAIN RFID reader. This circuitry potentially includes attenuators, one or more SAW filters, DC blocking series capacitors, one or more power amplifiers, one or more directional couplers, optional RF switches, and passive filters. All these components serve different purposes that are explained in detail in the Impinj E710 Development Board Application Note. A simplified example circuit is shown in Figure 18.

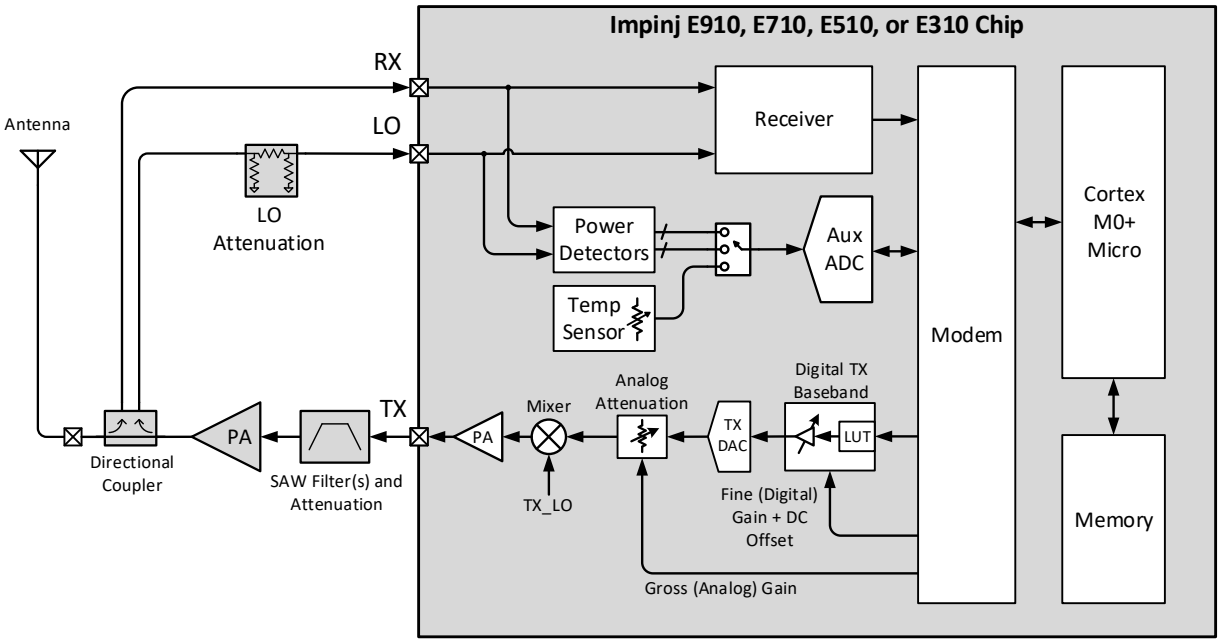
Figure 18 – RF Front End Block Diagram



3.5 RF Power Detection

The Impinj E910, E710, E510, and E310 reader chips contain power detectors connected to the RX and LO pins, allowing measurement of forward (transmit) power on the LO pin and reverse (self-jammer) power on the RX pin. These power detectors convert the RF power level at the RX and LO pins into analog voltages, which are measured by the Auxiliary ADC inside the reader chips. LO power measurements are used to measure the forward power for closed loop transmit power control via the fine gain in the transmitter. This arrangement is shown in Figure 19. These sensors require some calibration in circuit because circuit design and component values will alter the transfer function between the desired quantities and the power at the reader chip pins. For more detail on calibration and closed loop power control, see the Impinj E910, E710, E510, and E310 Based Reader Calibration Application Note.

Figure 19 – Impinj Reader Circuit Block Diagram With Sensors



3.6 Frequency Generation

3.6.1 Temperature Compensated Crystal Oscillator

The Impinj E910, E710, E510 and E310 reader chips require a high accuracy clock reference signal from an external temperature compensated crystal oscillator (TCXO) to be used as a reference for the voltage-controlled oscillator and phase-locked loop internal to the reader chip. The TCXO clock output signal is fed into the reader chip via the high impedance FREF pin. The FREF pin requires AC coupling to remove the DC bias voltage of the TCXO output. The Impinj E710 development board uses a 1 nF capacitor, but other TCXOs may require a different component value. Some TCXO components require a specific load to operate, and this may require external passive components to implement.

TCXO selections should meet the requirements listed in the electrical specifications, specifically Table 16, including the frequency, PPM error, and output waveform's shape and peak to peak voltage. If the peak-to-peak voltage exceeds the specifications of the reader chip, it can be reduced using a voltage divider circuit before the AC coupling capacitor. If necessary, Impinj recommends using a resistor voltage divider with a series resistance of 1 kΩ, and an appropriately scaled shunt resistance for the waveform amplitude. If the waveform shape is not a clipped sine wave, for example a CMOS or HCMOS square wave, it may need to be low-pass filtered using an RC circuit to reduce higher order frequency content, as these can couple into the transmitter and receiver and degrade performance. The TCXO power supply can likewise contain high frequency noise and may require some electrical isolation from the reader circuit.

An example TCXO circuit is shown in Figure 20.

Other TCXO specifications that may matter in the reader system include startup time, power consumption, frequency stability over time, voltage, temperature, and load, etc. These specifications must be considered in reader design, as they may have design implications.

Some TCXO devices are "pullable" meaning a voltage can be applied to one of their pins to shift the operating frequency. This may be used as a mechanism of frequency calibration. If this behavior is not desired, the pin should be driven to the appropriate DC value to disable frequency pulling.

Impinj has used the following TCXOs with success:

- TXC 7Q-24.000MBN-T
- Taitien TXEABLSANF-24.000000

- Abracon ASTX-H11-24.000MHZ-T
    - Note: Requires an output voltage divider to achieve <1.5 V_{P-P} input level
    - Impinj achieved this using a resistor voltage divider including 1 kohm series resistor and a 432 ohm shunt resistor, followed by a 1 nF series capacitor at the FREF pin

3.6.2 Voltage Controlled Oscillator

The Impinj E910, E710, E510 and E310 reader chips contain a voltage-controlled oscillator (VCO) that generates a ~3.6 GHz reference signal. The reference signal is subsequently divided by 4 to generate the carrier wave (CW) signal used for RF transmission, also known as the Transmit LO (Local Oscillator) signal. This reference signal is tunable, allowing the reader chips to operate in different channels in multiple regulatory regions. The VCO is tuned using closed loop feedback from the phase-locked loop (PLL), using the TXCO as a reference clock.

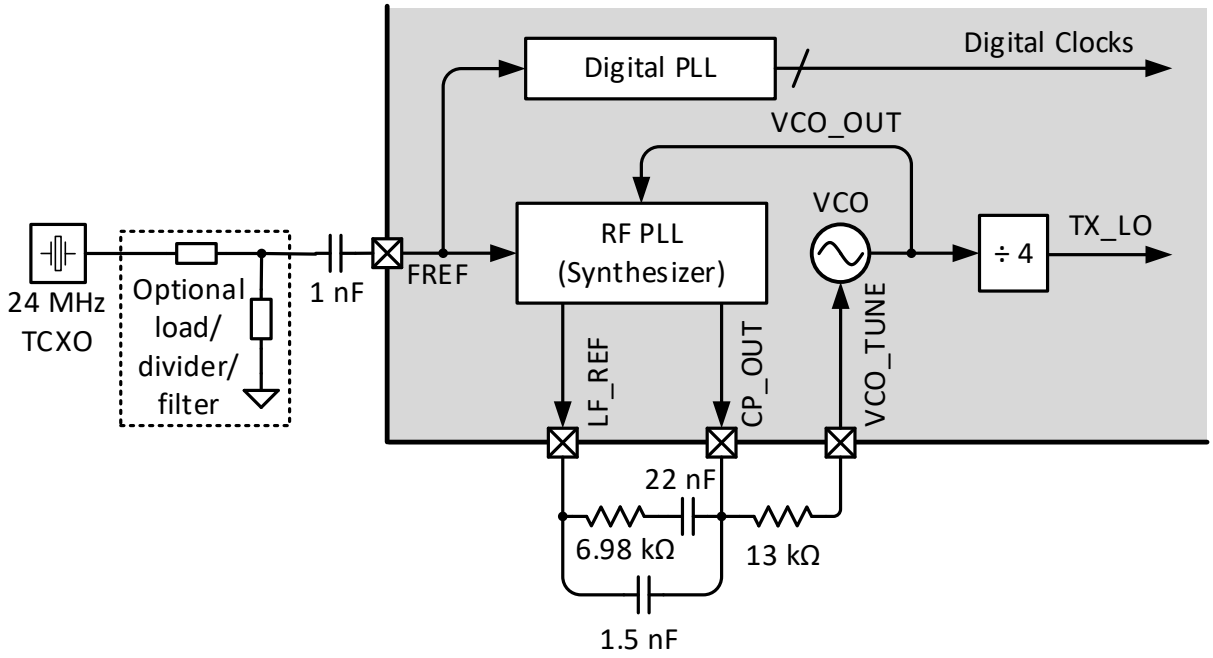
The VCO and phase-locked loop circuits are configured by the reader chips' embedded firmware image. The SPI host can interact with this configuration via Operations and Register values. This is demonstrated in the SDK's examples, as described in the Impinj Reader Chip SDK Documentation.

3.6.3 PLL Loop Filter

In addition to the VCO, the Impinj E910, E710, E510 and E310 reader chips have a built-in phase-locked loop (PLL) circuit, which allows automatic tuning of the VCO to a specific desired frequency, using the 24 MHz TCXO clock input as a reference. The PLL requires an external loop filter made up of passive components to provide optimum performance. The external TCXO output signal must also be connected to the FREF input as described above in section 3.6.1 - Temperature Compensated Crystal Oscillator. The recommended circuit components and topology are shown in Figure 20.

Impinj recommends that partners use the specific component values and tolerances that are used in the Impinj E710 development board. The BOM for the development board can be downloaded from our support portal here: https://support.impinj.com/hc/en-us/articles/360011416140

Figure 20 – PLL Block Diagram and Loop Filter Topology



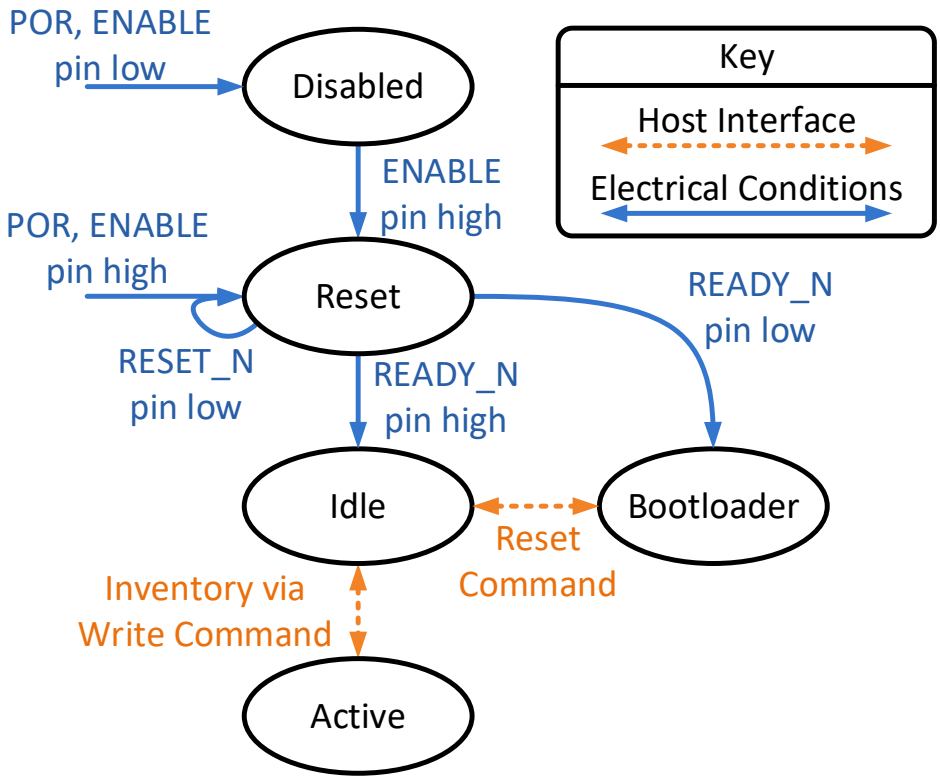
3.7 Power Modes

The Impinj E910, E710, E510, and E310 reader chips have multiple operating modes, allowing power consumption and performance optimizations for all applications. The power modes and transitions between them are shown in Figure 21. Power consumption characteristics of the modes are shown in Table 8.

When power is applied to all of the power supply pins on the reader chip, it will enter either Disabled or Reset power mode, depending on the state of the ENABLE pin. If the ENABLE pin is low, it will enter the Disabled mode, but if the ENABLE pin is high, it will enter the Reset mode. From the Reset mode, if the RESET_N pin is high, the reader chip will transition into either the Idle or Bootloader mode, depending on the state of the READY_N pin. The READY_N pin can be driven low to force the reader chip into the Bootloader mode or left high to allow the reader chip to boot into Idle mode. From Idle mode, the reader chip can be sent into the Active mode(where RFID operations are performed) or Bootloader mode, depending on commands sent via the host interface. The RESET_N pin can be used at any time to force the reader chip into the Reset mode or keep it there indefinitely. Setting the ENABLE pin low will force the reader chip into the Disabled power mode, which consumes less current than any of the other power modes. Refer to section 2.3 - Power Supply for details on power mode transitions.

The Impinj E910, E710, E510, and E310 reader chips do not have an independent internal clock source, and if no 24 MHz clock signal is provided at the FREF input, the parts will not start up.

Figure 21 – Impinj Reader Chip Power Modes



4 DEVICE CONTROL AND PROGRAMMING

The Impinj E910, E710, E510, and E310 reader chips have an embedded Cortex-M0 microcontroller that runs RAIN application specific firmware provided by Impinj. That firmware implements the behavior necessary to operate the RAIN radio and exposes an interface for communication with a host device. The host device communicates with the reader chip over an SPI channel, implementing a specific communication scheme that is explained further below. Impinj provides explicit documentation of the "wireline" details of the protocol, enabling users to implement their own code to communicate with the

reader chip. Impinj also provides an example implementation of a host library designed to communicate with the reader chip.

The Impinj E910, E710, E510, and E310 reader chips' embedded microcontrollers can only run the Impinj provided firmware images and will not execute any other application code. The reader chip exposes a firmware update interface(bootloader), so that newer versions of the firmware can be installed on the reader chip, adding new features, fixing bugs, etc. In addition to the RAIN behavior, the firmware also implements test and calibration functionality, and allows the non-volatile storage of calibration configuration, as well as stored configurations for RAIN behavior.

The Impinj E910, E710, E510, and E310 reader chips are populated with a firmware image during Impinj's manufacturing and test process. Impinj will populate with the latest major revision of firmware. The major revision is updated when large changes are made to the host interface, new reader chip devices are added, or major bugs are fixed. These major revision updates will be communicated to partners via PCN. Readers containing the Impinj E910, E710, E510, and E310 reader chips should include the capability to update the firmware image on the reader chip in the field, so that bugs can be removed, and new features can be added. Firmware updates should also be implemented during reader manufacturing flow, guaranteeing a specific firmware image version. For more information on performing firmware updates, see the Impinj Reader Chip SDK Documentation.

Further detail on the behavior of the embedded microcontroller is contained within the Impinj Reader Chip SDK Documentation. This document contains information on the structure of the data that is sent across the SPI communication interface, as well as the commands and responses that can be exchanged. It also contains a map of the registers that are used to read and write device configuration. It will document the functional behavior of the reader chip, including all the different operating modes the device supports.

4.1 Reader Communication Protocol

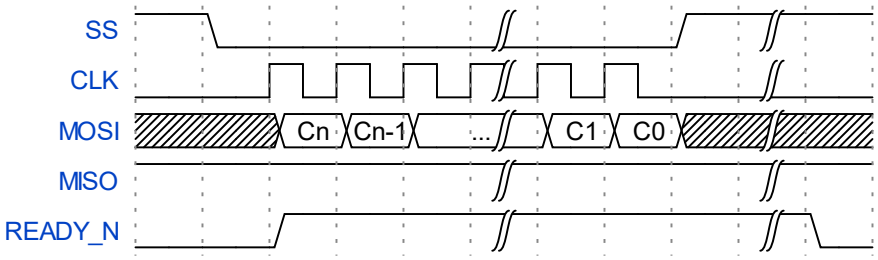
Impinj E910, E710, E510, and E310 reader chip communication with an SPI master host uses bytes that are sent across the SPI interface to build messages. These messages can describe commands from the host to the reader chip, and optionally responses from the reader chip to the host. Commands begin with a single "ID" byte, and responses begin with a single "response code" byte, and both are optionally followed by a payload made up of one or more fields of data, each broken up into a number of individual bytes. Not all commands have responses, but they will often change the state of the device registers. More detail on the reader communication protocol is contained in the Impinj Reader Chip SDK Documentation.

4.2 SPI Digital Communication Interface

The Impinj E910, E710, E510, and E310 reader chips communicate via SPI (Serial Peripheral Interface). The reader chip acts as an SPI slave. The reader chip has additional digital IOs that help coordinate SPI communication with the host, including the READY_N and IRQ_N pins.

The SPI uses 8-bit words, communicated most significant bit first. If multiple bytes are sent, they are sent with the most significant byte first. Both are "big endian". The SPI CPOL = 0, which means the clock signal SCLK idles low. The SPI CPHA = 1, which means the data pins MOSI and MISO states should change on the rising edge of the clock, and be sampled on the falling edge of the clock. For more details on the SPI timing parameters, see section 2.4.6. Some host devices may require a ~1k Ω pulldown resistor on the SCLK signal depending on their configuration.

Figure 22 – SPI Master Transaction With No Response



For more details on Impinj E910, E710, E510, and E310 reader chip SPI behavior and the host communication protocol, see the Impinj Reader Chip SDK Documentation.

4.3 Digital Input/Output Pins

The Impinj E910, E710, E510, and E310 reader chips have Digital Input/Output pins (DIGITAL_IOs) that can be used as digital inputs or outputs in certain configurations, for example for switching between antennas, SAW filters, or baseband receive filters, or reading external voltages. For more detail on controlling the Digital IOs, see the Impinj Reader Chip SDK Documentation.

5 PERFORMANCE CHARACTERISTICS

5.1 RX Sensitivity Summary

Receive sensitivity varies with many design parameters, including components used in the RF front end, the baseband filter, power supply topology, selected reader mode, etc. The RX sensitivity of the Impinj E710 development board has been captured in the Impinj E710 Development Board Application Note.

For more details on optimizing RX sensitivity, see the Impinj Reader Chip RF Performance Optimization Application Note.

5.2 Transmit Output Spectral Summary

Transmit output spectrum will vary by RF Mode (Link Profile) and external reader hardware. There is more detail on the transmit spectral performance in the Impinj E710 Development Board Application Note.

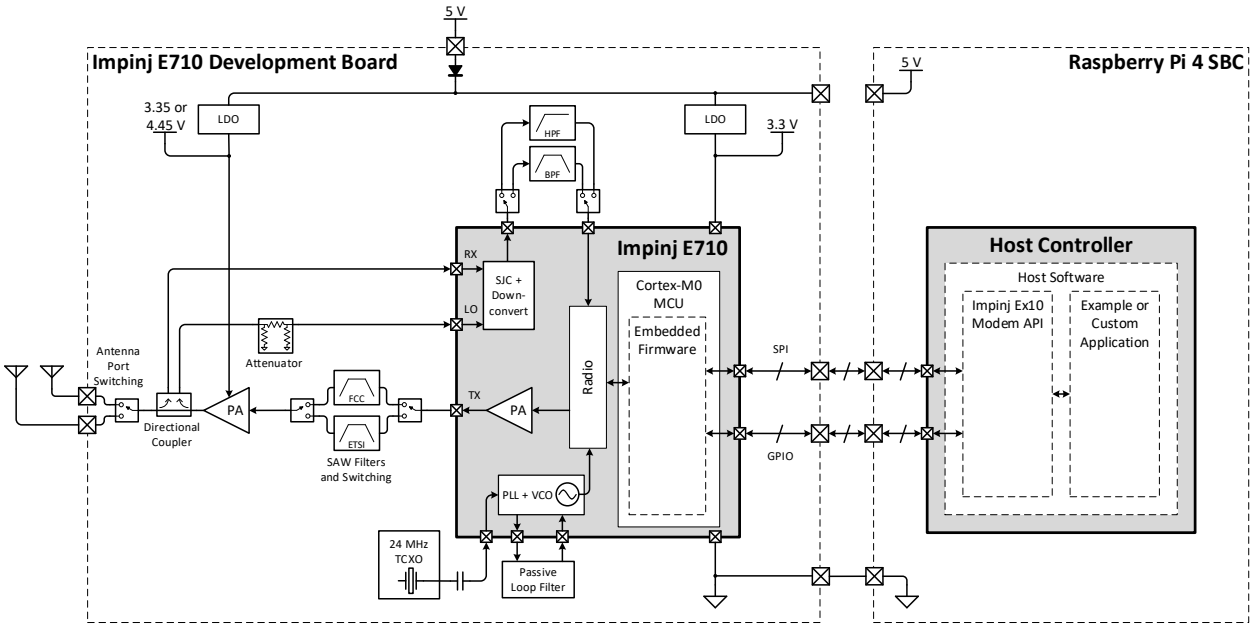
5.3 Transmit Power Control

The Impinj E910, E710, E510, and E310 reader chips have configurable transmit power gain, allowing run-time reconfiguration of the RAIN reader's transmit power. This system transmit power requires calibration to improve accuracy. For more detail on transmit power control and calibration, see the Impinj E910, E710, E510, and E310-Based Reader Calibration Application Note.

6 IMPINJ E710 DEVELOPMENT BOARD

For more application specific details on hardware configuration of the Impinj E910, E710, E510, and E310 reader chips, see the development board documentation, including the Impinj E710 Development Board Application Note. Figure 23 shows a detailed internal block diagram of the Impinj E710 development board and Raspberry Pi Host Single Board Computer (SBC).

Figure 23 – Impinj E710 Development Board System Detailed Block Diagram

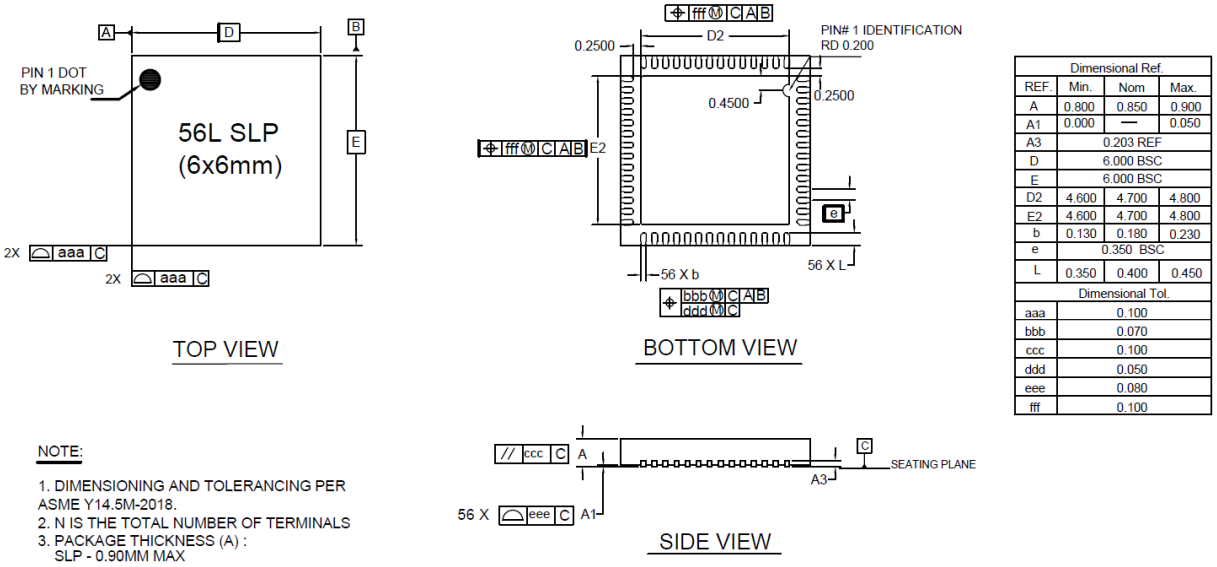


7 PACKAGE AND LAYOUT INFORMATION

7.1 Package Dimensions

The Impinj E910, E710, E510, and E310 reader chips are packaged in a 6 x 6 mm, 0.85 mm thick, 56-pin leadless sawn QFN package with a center e-pad that is connected to ground. The pins are spaced at a 0.35 mm pitch, center to center. The package and pin dimensions are shown in Figure 24.

Figure 24 – Impinj Reader Chip Package and Pin Dimensions



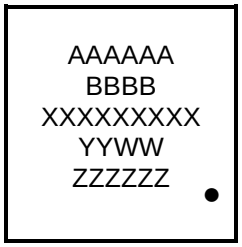
Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
A1	0.000	—	0.050
A3	0.203 REF		
D	6.000 BSC		
E	6.000 BSC		
D2	4.600	4.700	4.800
E2	4.600	4.700	4.800
b	0.130	0.180	0.230
e	0.350 BSC		
L	0.350	0.400	0.450
Dimensional Tol.			
aaa	0.100		
bbb	0.070		
ccc	0.100		
ddd	0.050		
eee	0.080		
fff	0.100		

Note: These dimensions describe the latest version of the package. Previous versions had slightly different package thickness and lead length specifications. For more details, see our Product Information Notification here: https://support.impinj.com/hc/en-us/articles/4418337492755

7.2 Package Markings

The markings on the Impinj reader chip package are shown in Figure 25 and enumerated in Table 21. Note the pin 1 marking is in the lower right corner, relative to the text.

Figure 25 – Impinj Reader Chip Package Markings



Note: Drawing is not to scale

Table 21: Impinj Reader Chip Package Markings Encoding

Field	Definition
AAAAAA	"IMPINJ" or "PI" depending on lot
BBBB	Reader Chip Model Number (e.g. "E710")
XXXXXXXXX	Lot Number
YYWW	Date code (year and workweek)
ZZZZZZ	Country of origin

7.3 PCB Layout Recommendations

7.3.1 Recommended PCB Footprint

Impinj has implemented a recommended PCB footprint in our Impinj E710 Development Board, the Altium source for which can be downloaded from our support portal here: https://support.impinj.com/hc/en-us/articles/360011416140

Impinj's recommended footprint pad dimensions are shown in Figure 26 and solder paste dimensions are shown in Figure 27.

Figure 26 – Recommended PCB Footprint Pad and Soldermask Dimensions

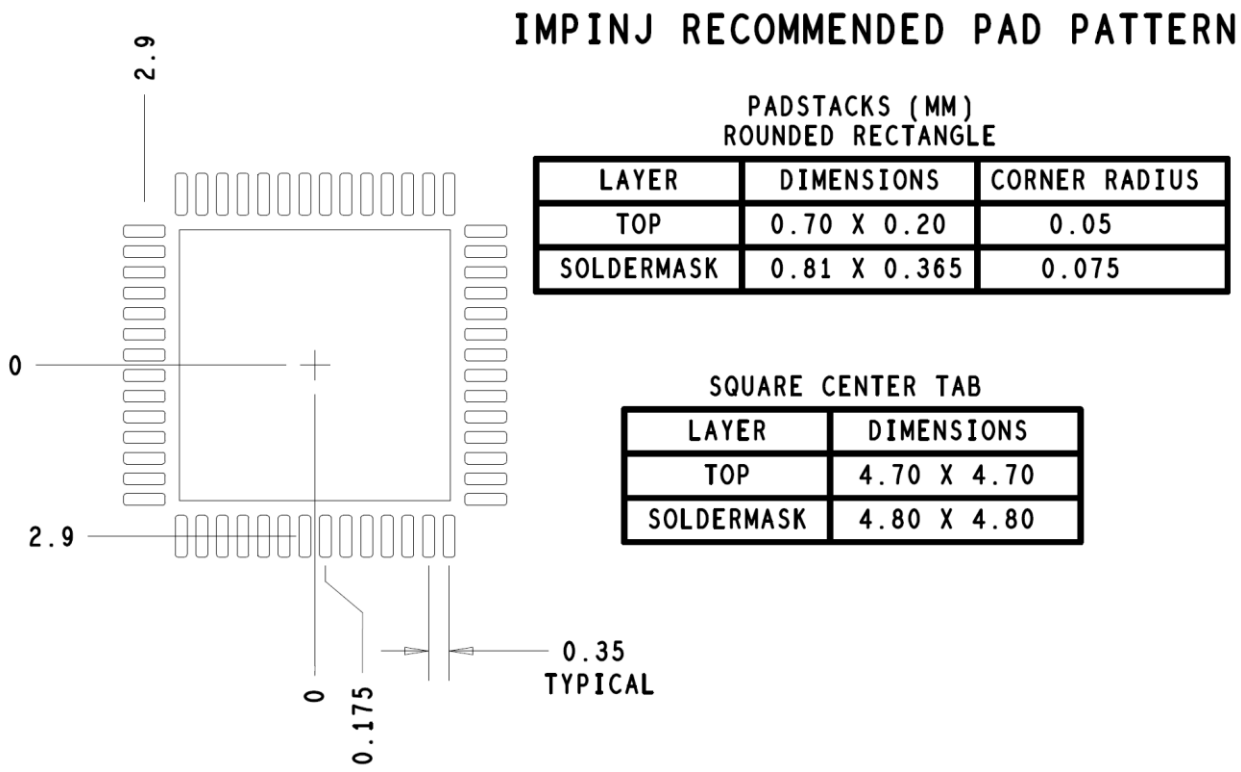
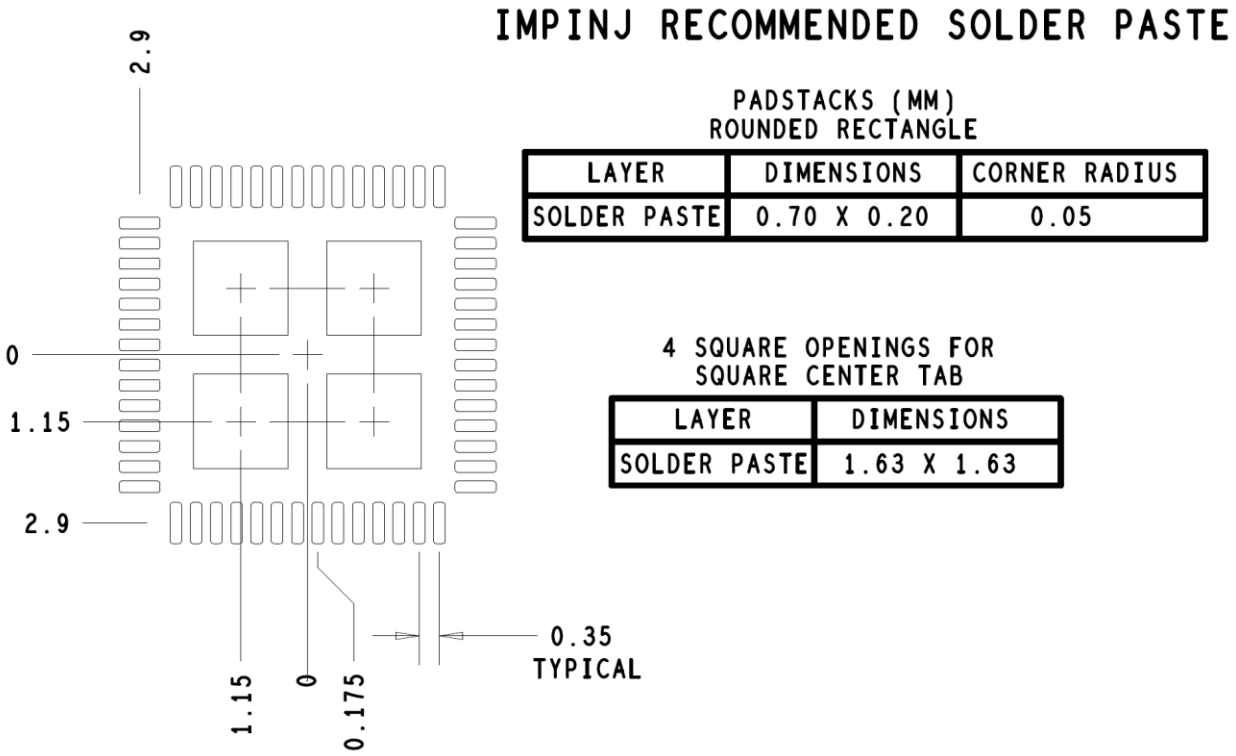


Figure 27 – Recommended PCB Footprint Solder Paste Dimensions



7.3.2 Additional PCB Layout Recommendations

Radio circuit performance can vary widely depending on the routing of signals on the PCB. This section contains a series of recommendations to optimize PCB layout.

The RF signal paths of the radio circuit (including the TX, LO, and RX signals) should all be made up of 50-ohm characteristic impedance traces. This will minimize signal reflections and optimize reader efficiency and sensitivity. Although the baseband filter has a characteristic impedance, the signal frequencies are low enough that the traces do not need to be controlled impedance. The three signal paths should also be isolated from each other and from other signals on the PCB as much as possible, separated by ground fills on all possible layers.

PCB layout has a large impact on thermal circuit performance. The electrical conductivity of the traces, vias, and fills that make up the layers of a PCB also makes them very thermally conductive. Both the PA and Impinj E910, E710, E510, and E310 reader chips will self-heat as they consume electrical power. The reader chip and most PA components have large ground paddles or multiple ground pins to help conduct heat out of the ICs. These pins and paddles should be thermally and electrically connected to the ground fills of the reader board, using a healthy number of vias to cross from layer to layer where necessary. To further improve thermal performance in high-power applications, the ground fills of the reader PCB should be connected to a heat sink or chassis for dissipation into the surrounding environment.

All of the ground leads on the Impinj E910, E710, E510, and E310 reader chips, including the RF TX_GND, LO_GND, and RX_GND, should be tied directly to the PCB's ground net, via direct traces to the large thermal and electrical ground paddle corresponding to the e-pad in the center of the QFN package. This will ensure optimal RF, electrical, and thermal performance.

For an example of optimal layout for an Impinj E910, E710, E510, or E310 based RAIN RFID reader circuit, and more PCB layout guidance, see the Impinj E710 Development Board Application Note.

7.4 Recommended Reflow Profile

Impinj recommends a JEDEC standard J-STD-002D profile with a peak temperature of between 245° C and 250° C, with the characteristics listed in Table 22.

Table 22: Recommended Reflow Profile Parameters

Parameter	Min	Typ	Max	Unit
Temperature Ramp Up Rate			3	° C / second
Preheat Temperature	150		200	° C
Preheat Time	60		180	seconds
Liquidus Temperature		217		° C
Time above Liquidus Temperature	60		150	seconds
Peak Temperature	245		250	° C
Time within 5° C of Peak Temperature	20		40	seconds
Temperature Ramp Down Rate			6	° C / second
Time Between Room Temp and Peak Temperature			480	seconds

8 TERMINOLOGY

Table 23 contains a list of relevant terminology and acronyms specific to RF systems and RAIN embedded readers.

Table 23: Relevant Terminology

Term	Definition
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
AUX	Auxiliary
BLF	Backscatter Link Frequency / Backward Link Frequency
BPF	Band Pass Filter
CW	Continuous Wave (Pure sine wave transmitted by reader when listening to tags)
DAC	Digital-to-Analog Converter
DRM	Dense Reader Mode
DSB	Double Sideband
EOT	End of Transfer
EPC	Electronic Product Code
FCC	Federal Communications Commission (US Regulatory Body)
FIFO	First In, First Out
FIR	Finite Impulse Response
I	In-phase
IF	Intermediate Frequency
IIP	Input Intercept Point
IIR	Infinite Impulse Response
I-Q	In-phase Quadrature
ISM	Industrial, Science, and Medical
ISO	International Standards Organization
ISO18000	Tags and Readers conforming to ISO/IEC FDIS 18000-6:2003(E)
LBT	Listen Before Talk
LFSR	Linear Feedback Shift Registers
LNA	Low Noise Amplifier
LO	Local Oscillator
LUT	Lookup Table
MSB	Most Significant Bit
PA	Power Amplifier
PER	Packet Error Rate
PLL	Phase Locked Loop
POR	Power On Reset
PR	Phase Reversal
Q	Quadrature-phase

Term	Definition
RAIN	UHF Gen 2 RFID
RF	Radio Frequency
RFID	Radio Frequency Identification
RSSI	Received Signal Strength Indicator
RX	Receiver
S11	Input reflection coefficient S-parameter
SJ	Self Jammer — also known as Tx carrier present at the RX, typically from antenna reflection
SJC	Self Jammer Cancellation — circuitry that removes SJ from RX port
SPI	Serial Peripheral Interface
TX	Transmitter
TCXO	Temperature Compensated Crystal Oscillator
UHF	Ultra High Frequency (~900 MHz)
VCO	Voltage Controlled Oscillator

9 REFERENCE DOCUMENTS

Related documents are listed in Table 24. All documents can be downloaded from the Impinj support portal here: https://support.impinj.com/hc/en-us/sections/360003305060

Table 24: Reference Documents

Document	Description
Impinj E710 Development Kit User's Guide	Documents how to use the Impinj E710 development kit, Impinj reader chip SDK, and host examples, including Quick Start Guide.
Impinj Reader Chip SDK Documentation	Documents the interfaces between the host and the Impinj reader chips, including the SPI wireline, messages, registers, and FIFOs.
Impinj E710 Development Board Application Note	Documents the Impinj E710 development board hardware, circuit topologies, design performance, and potential modifications.
Impinj Reader Chip Datasheet **(this document)**	Documents the Impinj E910, E710, E510, and E310 reader chips, including electrical and mechanical specifications.
Impinj Reader Chip RF Performance Optimization Application Note	Documents how to measure and optimize RF performance in Impinj Reader Chip-based RAIN RFID reader devices.
Implementing an MCU host with the Impinj E710 development board	Demonstrates porting the Impinj reader chip C host library to an MCU and implements a simple inventory reader application.
Impinj E910-, E710, E510, and E310-Based Reader Calibration Application Note	Documents an example procedure and background to calibrate an Impinj reader chip-based RAIN RFID reader.

10 DOCUMENT CHANGE LOG

Table 25: Document Change Log

Version	Date	Description
1.0	2021-05-27	• First production version of this document. For details on preliminary changes, please contact support@impinj.com
1.1	2021-12-06	• Added tag read rate to overview in Table 1 • Added section 2.4.6 - Host SPI Interface Functional Specifications • Updated RF modes and tag read rates for FW v1.1 in Table 1, Table 10 and Table 12 • Increased maximum power consumption specs in Table 8 • Populated RSSI Accuracy and Phase Measurement Accuracy specs in Table 13 • Removed “TBD” TX Spurious Emissions spec from Table 16 • Populated Auxiliary ADC INL spec in Table 17 • Added part markings in section 7.2 • Added recommended reflow profile in section 7.4
1.2	2022-02-28	• Added a note below Figure 24 to clarify dimensions of chips from all assembly vendors • Updated Figure 25 and Table 21 to match markings from all assembly vendors

1.3	2022-06-27	• Added Impinj E910 reader chip throughout datasheet
		• Renamed Pin 29 to “STARTUP/DIGITAL_IO[6]” in Table 3
		• Added section 2.2.1 - Digital IO Default Drive Modes
		• Added internally regulated voltages to section 2.3 and Figure 4
		• Added new FW v1.2 reader mode 202 in Table 12
		• Clarified that reader mode sensitivity specs in Table 12 are at typical Gen2 parameter values
		• Increased LO and RX Pin maximum operating power specs in Table 13
		  ○ Impinj E710, E510, and E310 LO pin operating power spec increased to +18 dBm max
		  ○ Impinj E710, E510, and E310 RX pin operating power spec increased to +11 dBm max
		• Added more detailed drawings of recommended PCB footprint dimensions in section 7.3.1
		• Clarifications throughout

1.4	2023-08-24	• SDK+FW v2.0 updates ○ Added new reader modes to Table 12: Impinj Reader Chip Reader Mode Performance • Fixed a typo in section 2.3.1 about the READY_N condition for entering bootloader mode • Clarified startup sequence in section 2.3.1 • Added SPI parameters in section 2.4.6 • Added additional thermal data to Table 7: Chip Operating Conditions • Added reader mode list in Table 11: Impinj Reader Chip Reader Mode IDs and Parameters • Re-worded RX sensitivity spec in Table 12: Impinj Reader Chip Reader Mode Performance

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